INTERSIL

Using the Power MOSFET as a Switch

MOSFET STRUCTURES

A variety of structures for implementing a power MOSFET have been proposed and fabricated. Of these, only two structures, the flat-bottomed V-groove and the vertical DMOS (double-diffused MOS) structures, are currently available as viable power switches. A cross-section view of a V-groove device is shown in Figure 1. Fabrication of an n-channel device begins with an N^- epitaxial layer grown on an N^+ substrate. P and N regions are then diffused in, a flat bottomed groove is anisotropically etched into the surface, and then an insulated gate structure is deposited. The source metalization is connected to both the N and P diffused regions, thereby effectively shorting the base and emitter of the parasitic NPN transistor. The user should, however, keep in mind the presence of this parasitic NPN transistor, which in some circumstances will participate in the circuit operation. This will be treated in later sections.

DMOS devices are very similar to V-groove (or VMOS) devices except that no groove is used and the gate structure is planar (Figure 2). Manufacturers have given the DMOS devices a variety of names, such as HEXFET, TMOS, XMOS, ZMOS, etc. These are all basically the same structure, with variations in the shape of the P diffusions and the cell interconnections.

Inherent in the MOSFET structure are voltage variable capacitances and resistances. The ON resistance is the sum of the epitaxial region resistance, the channel resistance, which is modulated by the gate-source voltage, and the lead and connection resistances. In addition there is a small but definitely non-zero resistance, r_{BE}, between the base and emitter of the parasitic transistor due to the bulk resistance of the structure.

Most MOSFETs use a form of silicon gate structure where the gate and the connection to the gate is made with doped silicon. The SiP material, while very useful in the structure, has a resistivity about 3,000 times greater than aluminum, and in some devices creates a substantial resistance in series with the gate.

Capacitance exists within the structure from the gate to the source, C_{gs}, the gate to the drain, C_{gd}, and from the drain to the source, C_{ds}. C_{ds} is essentially the capacitance of the base-emitter junction (C_{ob}) of the parasitic transistor and has the voltage-dependent characteristic typical of a PN junction. C_{gs} is relatively independent of voltage but the C_{gd} characteristic is very similar to C_{ds}.

The parasitic transistor also contributes capacitances. C_{ob} is equal to C_{ds}, since the same structure is involved. In addition, the base-emitter junction displays a typical diode junction characteristic.

P-channel MOSFETs are very similar to N-channel except that the N and P regions are interchanged. In P-channel devices the ON resistance for a given die area will be approximately twice that of a comparable N-channel device. The reason for this is that in the N-channel device the majority carriers are electrons but in the P-channel device the majority carriers are holes which have lower mobility. If the area of the P-channel device is increased to produce an equal $r_{DS(ON)}$ then the capacitance of the P-channel device will be higher and the device cost will also be greater. For this reason N-channel devices are usually preferred for power switches as long as the external circuits do not become overly complex to accommodate the N-channel device.

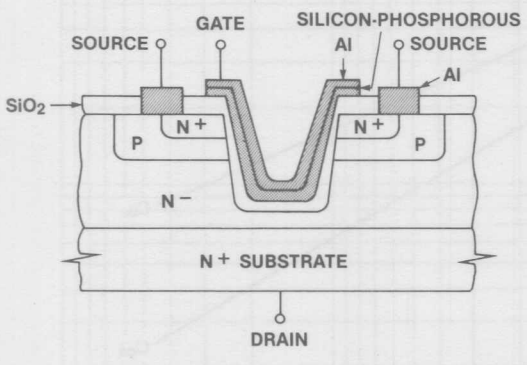

Figure 1. V-Groove MOSFET

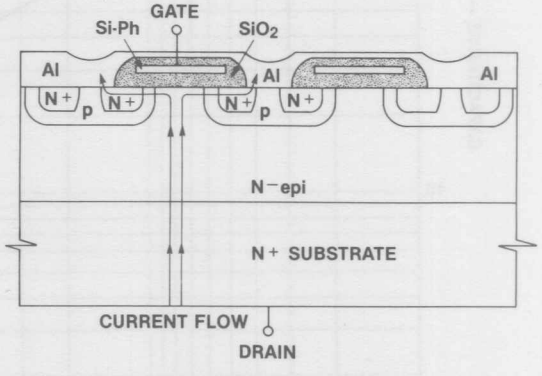

Figure 2. Vertical (DMOS) MOSFET

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SWITCHING CHARACTERISTICS

One of the major advantages of the MOSFET is its ability to switch very fast. Figure 3 shows a turn-on transition for an IVN6000 switching 350 volts in 5 nanoseconds! Most of the presently available power MOSFETs are capable of switching in a few nanoseconds **if** properly driven. Except for switching times of ten nanoseconds or less, the transition times are almost completely determined by the circuit in which the device is used. This is quite different from a bipolar junction transistor, where the physics of the device limit the switching speeds and no amount of drive wizardry will significantly improve things beyond a certain point.

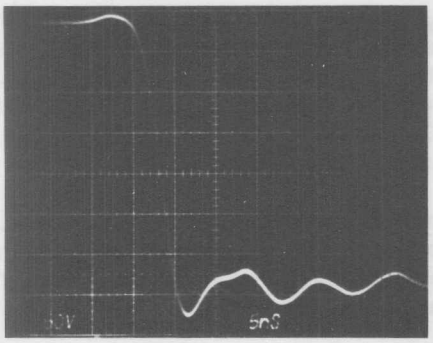


Figure 3. IVN6000 Turn-On

Capacitive Characteristics

For switching times down to about 10ns a MOSFET, from a drive point of view, is essentially a capacitor made up of C_{gs}, C_{gd} and C_{ds} as shown in Figure 4. A small signal measurement of these capacitances as a function of drain-source voltage, V_{DS}, for a typical device, is given in Figure 5. C_{gs} varies little with voltage, remaining about 210pF. C_{ds} and C_{gd} however are strong functions of voltage; C_{gd} is 400pF at 0 volts but decreases to 5pF at 350V, and C_{ds} also

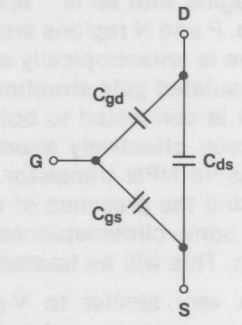


Figure 4. Capacitive Equivalent Circuit

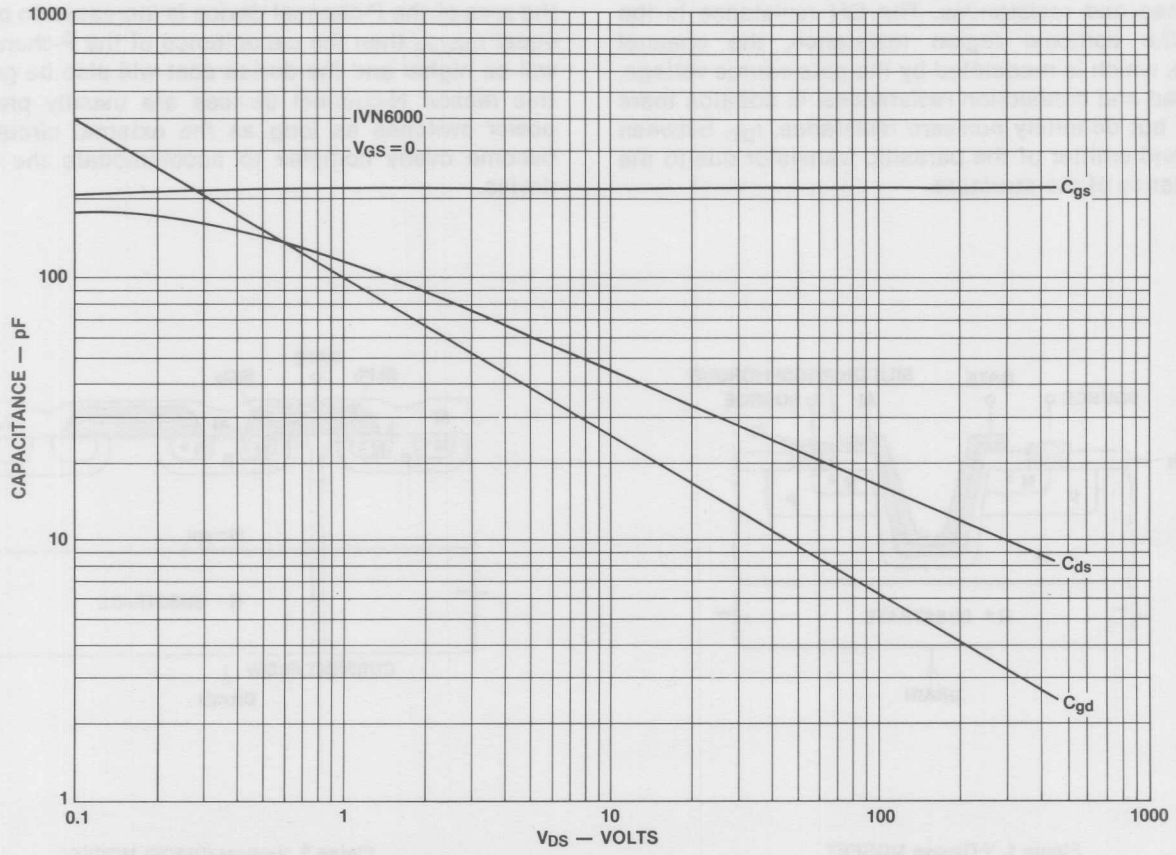


Figure 5. Capacitance Variation with Drain-Source Voltage

has a large variation. The small signal capacitance is interesting to a linear designer, but when the device is used as a switch the designer needs to know the large signal behavior. A much better way to present the data is shown in Figure 6 where the gate charge is plotted as a funtion of the gate-to-source voltage, V_{GS}, with the supply voltage, V_{DD}, as a parameter and the drain current, I_D, as a constant to represent the usual inductive load. Figure 7 shows a simplified version of the test circuit.

The curves in Figure 6 display three distinct operating regions. Region I is where V_{GS} is below the threshold voltage, V_{th}, so that the device is cut off and the capacitance is dominated by C_{gs}. For this device the small signal $C_{gs} = 210pF$, which is consistent with the Region I slope. Region II occurs as the device is turning on and represents the Miller capacitance, defined by:

$$C_m = -A_V C_{gd} \quad (1)$$

where:

$$A_V = -\frac{\Delta V_{DS}}{\Delta V_{GS}} \simeq -g_m R_L \quad (2)$$

Combining (1) and (2):

$$C_m \simeq g_m R_L C_{gd} \quad (3)$$

In the example shown in Figure 6, C_m is about 70nF. This large value occurs because of the current source in the drain lead; i.e., R_L is very large. When a lower impedance load is used in the drain, C_m will be much smaller and the slope of the Q_G/V_{GS} curves will be greater. The amount of charge required to charge C_{gd} is, however, a function of V_{DS} and not R_L or g_m, so that ΔQ_G for the Region II will increase with V_{DS}, displacing the curves to the right as shown. For a given V_{DD}, Q_G will not vary significantly with R_L. C_{gd} does vary slightly with variations in I_D and this would alter ΔQ_G with differing R_L values, but the effect is so small as to be of no practical interest in switching applications.

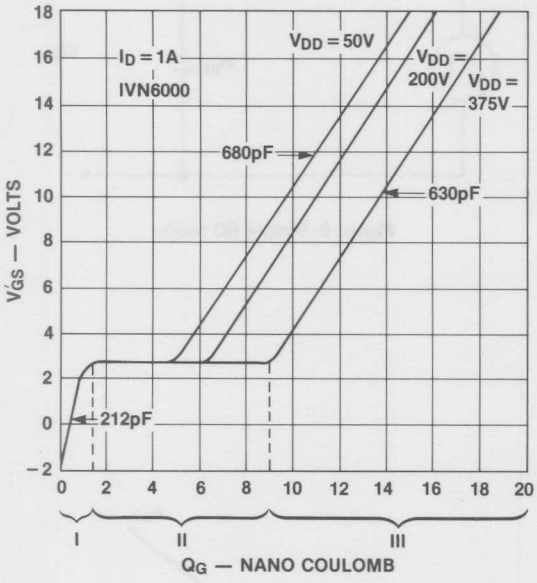


Figure 6. Gate Dynamic Characteristics

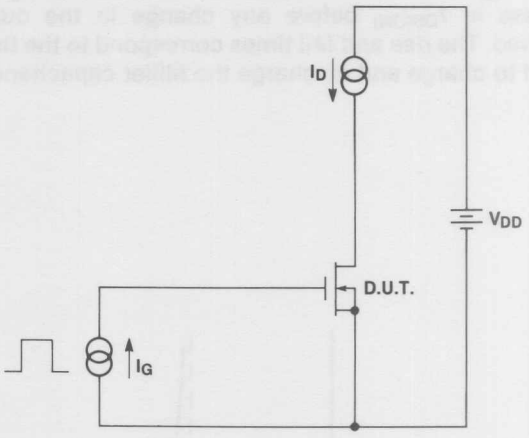


Figure 7. Simplified Test Circuit

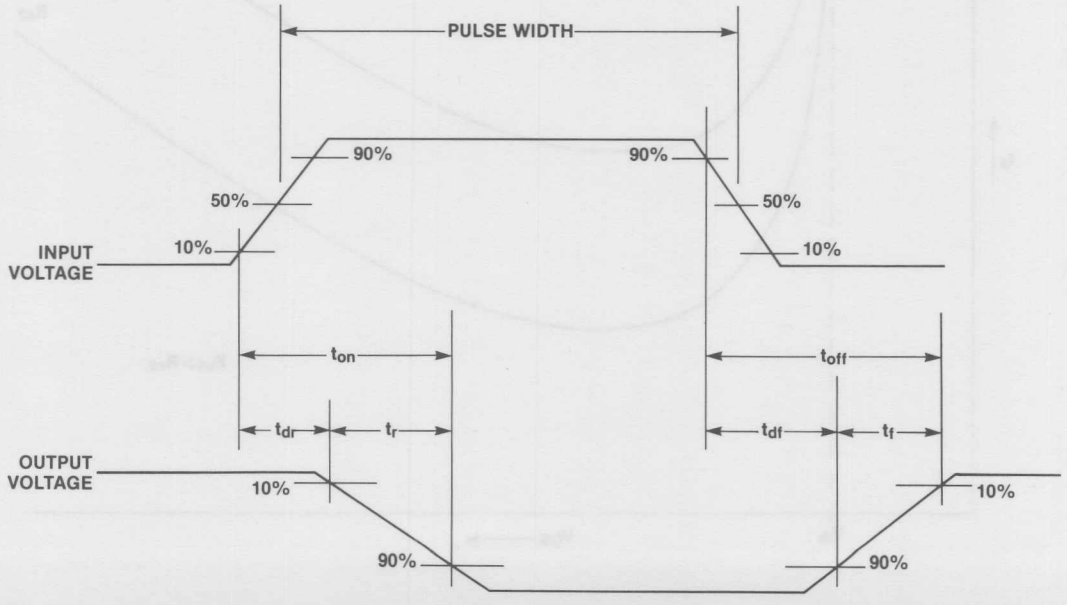


Figure 8. Switching Waveform

Region III represents operation with the device fully ON and V_{DS} near zero. Note that the capacitance in Region III is essentially the sum of C_{gs} and C_{gd} at low voltages, or about 650pF.

This set of curves can be used directly by the designer to determine both the switching time for a given drive impedance and the drive power. The drive power, P_d, for a resistive drive source and a switching frequency of f_o is

$$P_d = \Delta Q_G V_{GS} f_o \quad (4)$$

The effective input capacitance, C_{in}, for a given V_{GS}, is

$$C_{in} = \frac{\Delta Q_G}{\Delta V_{GS}} \quad (5)$$

The idealized switching waveforms are shown in Figure 8. A good approximation[1] for the switching times can be obtained from a piecewise linear approximation and a simple RC model (Figure 9) using the appropriate values for C_{in} in Regions I, II, or III. The turn-on delay, t_{dr}, represents the time required to charge C_{in} to $V_{GS} = V_{th}$, at which point the device begins to conduct. A similar delay time, t_{df}, exists at turn-off where V_{GS} must fall to the point where there is a significant increase in $r_{DS(ON)}$ before any change in the output is observed. The rise and fall times correspond to the times required to charge and discharge the Miller capacitance.

The total switching time, t_s, is defined as:

$$t_s = t_{dr} + t_r + t_{df} + t_f \quad (6)$$

If t_s is plotted as a function of the gate drive voltage for constant source resistance, curves like those shown in Figure 10 will be obtained. Thus, the designer is faced with a tradeoff. If large V_{GS} is used then t_{dr} and t_r will be short and $r_{DS(ON)}$ will be a minimum. Unfortunately, t_{df} becomes large, and t_s increases as does the drive power. If a small value of V_{GS} is used then t_{dr} and $r_{DS(ON)}$ increase rapidly. If both low $r_{DS(ON)}$ and minimum t_s are required then a value of V_{GS} that gives a satisfactory value of $r_{DS(ON)}$ must be used, and a sufficiently low value of R_S must then be selected to give the desired t_s.

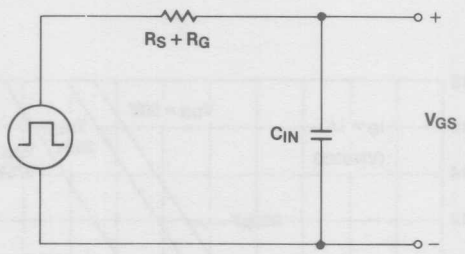


Figure 9. Simple RC Model

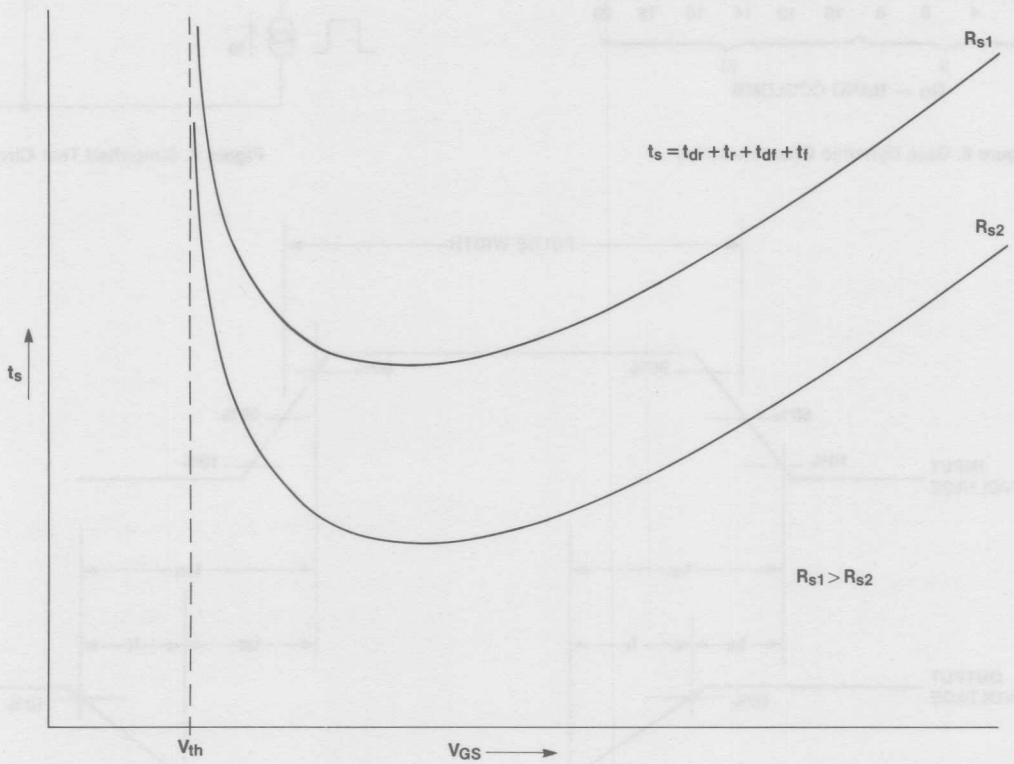


Figure 10. Total Switching Time as a Function of Gate Drive and Source Resistance

High-Speed Limitations

For very fast switching times (< 10ns) the simple RC model of Figure 9 is no longer adequate. The gate resistance, R_G, and the package inductances, L_S, L_G, and L_D, must be included, specially in large devices as shown in Figure 11. It is the parasitic inductances and gate resistances that limit the achievable switching speeds. For an IVN6000 device the minimum turn-on time is about 4ns.

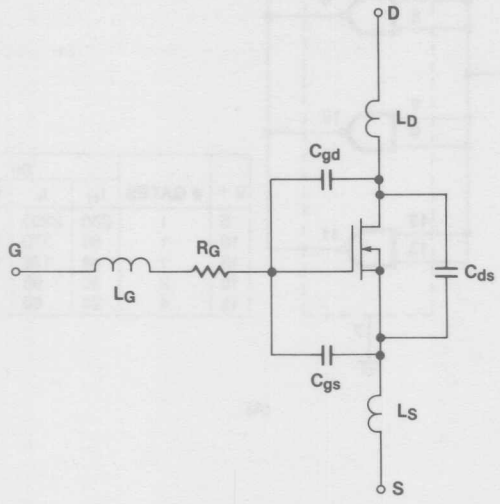
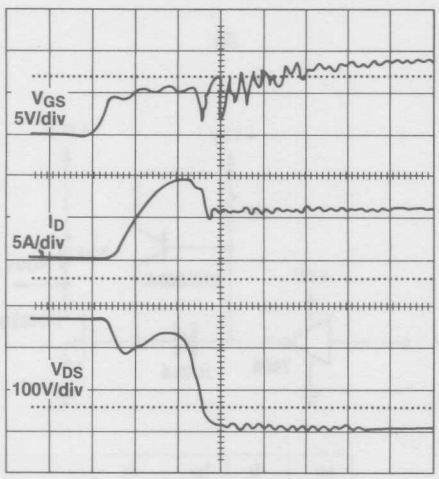


Figure 11. Equivalent Circuit Including Package Inductance and Gate Resistance

It has been shown[2] that inductance which is common to both the load and drive circuit, such as the source lead inductance or the wiring inductance, can produce a turn-on plateau in V_{DS} like that shown in Figure 12. The voltage, V_{SL}, across the common inductance, L_S, is:

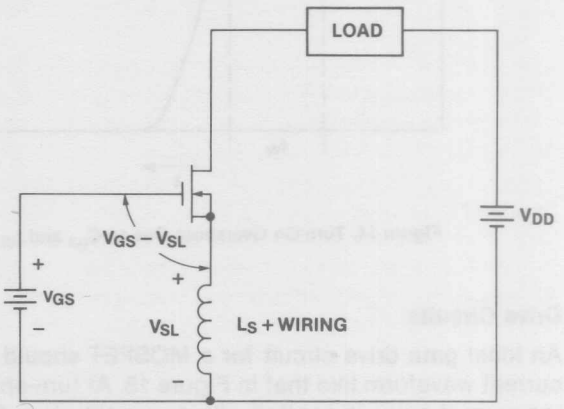
$$V_{SL} = L_S \left(\frac{dI_D}{dt} + \frac{dI_G}{dt} \right) \quad (7)$$



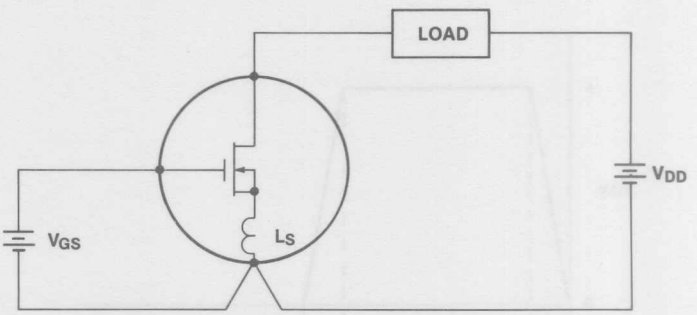
(Courtesy Duke University, Center for Solid-State Power Conditioning and Control)

Figure 12. Turn-On V_{DS} Plateau Due to L_S

This voltage subtracts from V_{GS} during the turn-on as shown in Figure 13A, restricting the gate enhancement. This effect can greatly increase the switching power loss because of the delayed fall of V_{DS} during turn-on. The problem can be minimized by separating the drive and load current loops right up to the device case as shown in Figure 13B. A TO-3 package will have an L_S of 1 to 10nH depending on the bonding wire size and the number of bond wires. Except for very high-speed or high-current applications this is not usually a problem, but even a small length of common external wiring can greatly increase the effective L_S and create a problem.



(A)



(B)

Figure 13

The drain-source capacitance, C_{ds}, can cause asymmetrical transition time between turn-on and turn-off even if the gate drive is perfectly symmetrical. At turn-on C_{ds} is discharged through $r_{DS(ON)}$ and the time constant is very short. At turn-off however the rate of voltage rise on C_{ds} is determined by the load, not by the switch. For a clamped inductive load with a large I_D at turn-off, C_{ds} will be charged quickly and there will be little difference between the gate and drain switching times, but if a resistive load is present the voltage across C_{ds} will have an exponential characteristic, with the load resistance determining the RC time constant. Even though the channel is turned off quickly V_{DS} may change slowly.

As shown in Figure 14, C_{gd} can cause pulse distortion during turn-on. During the interval when $V_{GS} < V_{th}$ (t_{dr}) the device is essentially a capacitor comprised of $C_{gd} + C_{gs}$, and the positive edge of V_{GS} is coupled to the output producing the initial positive pulse shown. A similar negative pulse can occur during the turn-off delay time.

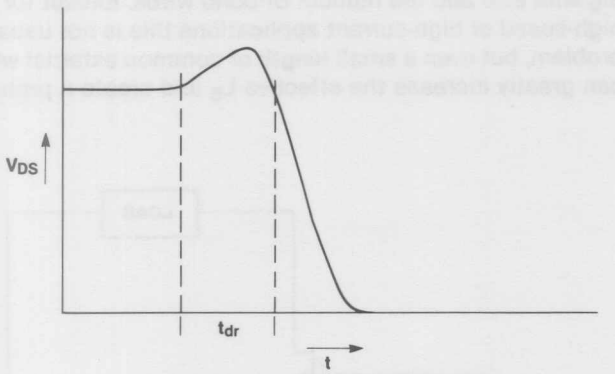


Figure 14. Turn-On Overshoot Due to C_{gd} and t_{dr}

Drive Circuits

An ideal gate drive circuit for a MOSFET should provide a current waveform like that in Figure 15. At turn-on a fast rising current pulse is applied with an amplitude sufficient for the desired rise time. When the desired value of V_{GS} is reached, I_G is reduced to the small value required to maintain V_{GS}. A typical MOSFET will have a gate current of less

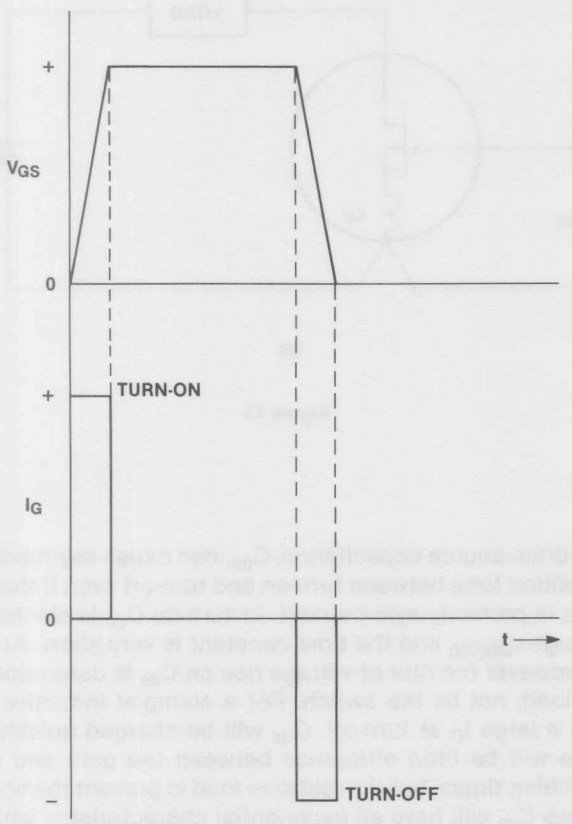
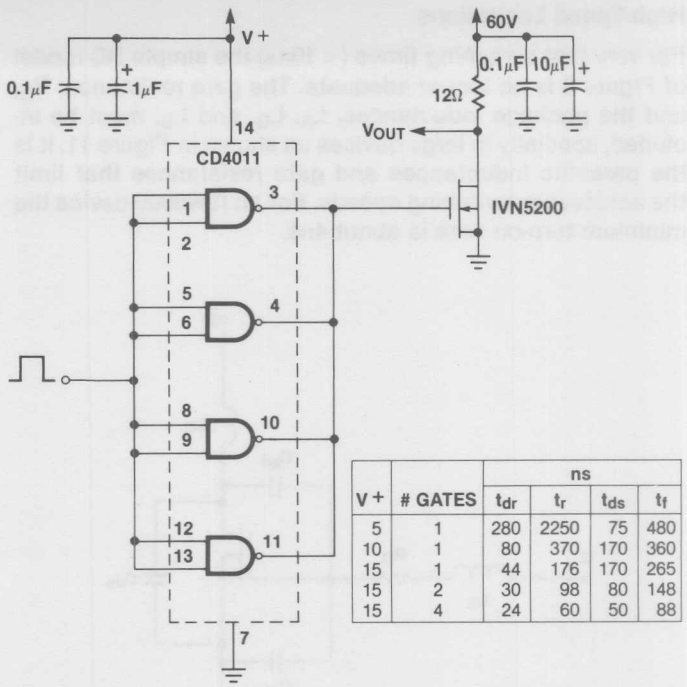
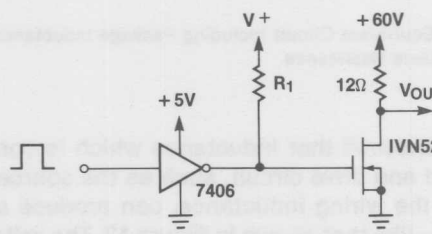


Figure 15. Ideal Gate Drive Waveforms



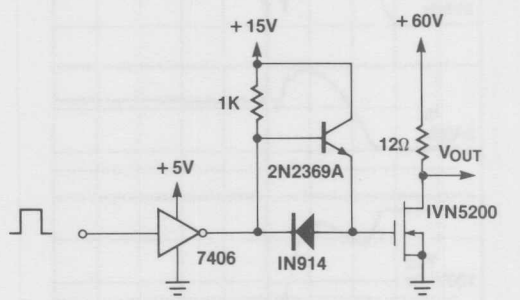
V+	# GATES	ns			
		t_{dr}	t_r	t_{ds}	t_f
5	1	280	2250	75	480
10	1	80	370	170	360
15	1	44	176	170	265
15	2	30	98	80	148
15	4	24	60	50	88

(A)



V+	R_1	ns			
		t_{dr}	t_r	t_{df}	t_f
15	390Ω	40	200	72	120
15	750Ω	40	340	70	110
30	750Ω	40	150	70	116
30	1.5K	66	290	64	100

(B)



t_{dr}	t_r	t_{df}	t_f
30ns	60ns	76ns	110ns

(C)

Figure 16. CMOS and TTL MOSFET Gate Drive Circuits

than 1nA but there may be other shunt elements (transformer magnetizing current, for example) in the gate circuit that require steady-state current. At turn-off a negative pulse is applied until V_{GS} is zero. As will be demonstrated shortly in the dV_{DS}/dt discussion, it is imperative that during the off time the gate-to-source impedance be as small as possible.

A close approximation to the ideal waveforms can be achieved with a variety of circuits. The simplest drive scheme is to use either CMOS or TTL buffers or gates as shown in Figure 16. These drive schemes are very attractive because of their simplicity, but the switching times are relatively slow due to the buffer output limitations. If greater speed is needed some form of low impedance bidirectional driver is needed; several such circuits are given in Figures 17 and 18. The DS0026 (Figure 17B) driver is particularly useful. This IC was designed as a NMOS clock driver to drive capacitive loads. There are two buffers in each package, each capable of sourcing or sinking 1.5 amperes with a switching time of 20ns. The DS0026 can be driven from TTL or CMOS logic. If the output from the DS0026 is not adequate, the output can be buffered with MOSFETs as shown in Figure 18A to provide much higher currents with no loss of speed. Figure 18B shows another driver that does not use a DS0026. If the two separate power supplies required in Figures 18A and 18B are not available, then the bootstrap versions in Figure 18C and 18D can be used.

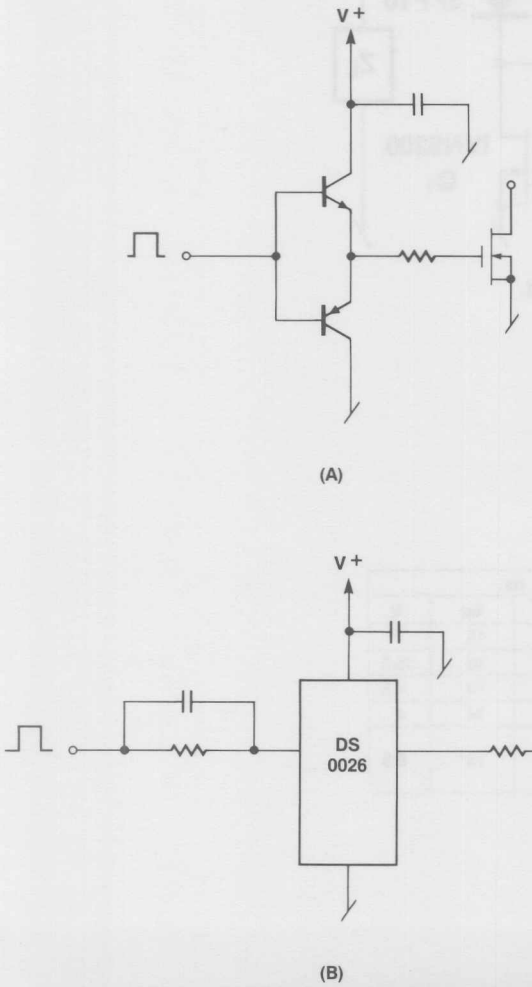


Figure 17. Bi-Directional MOSFET Gate Drive Circuits

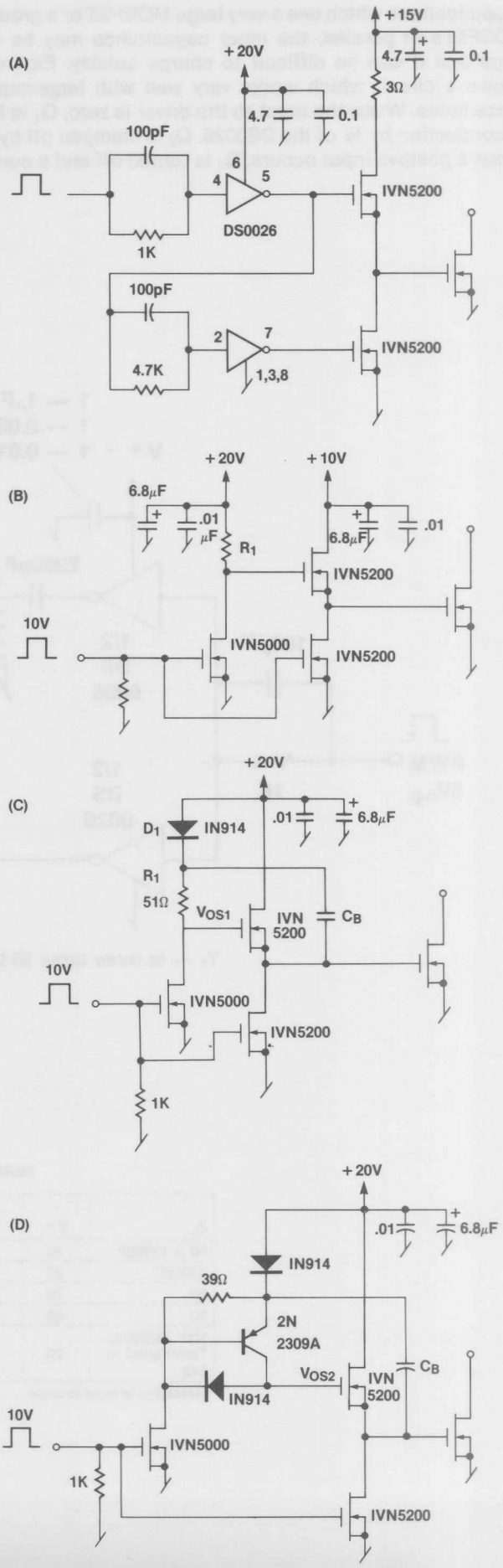
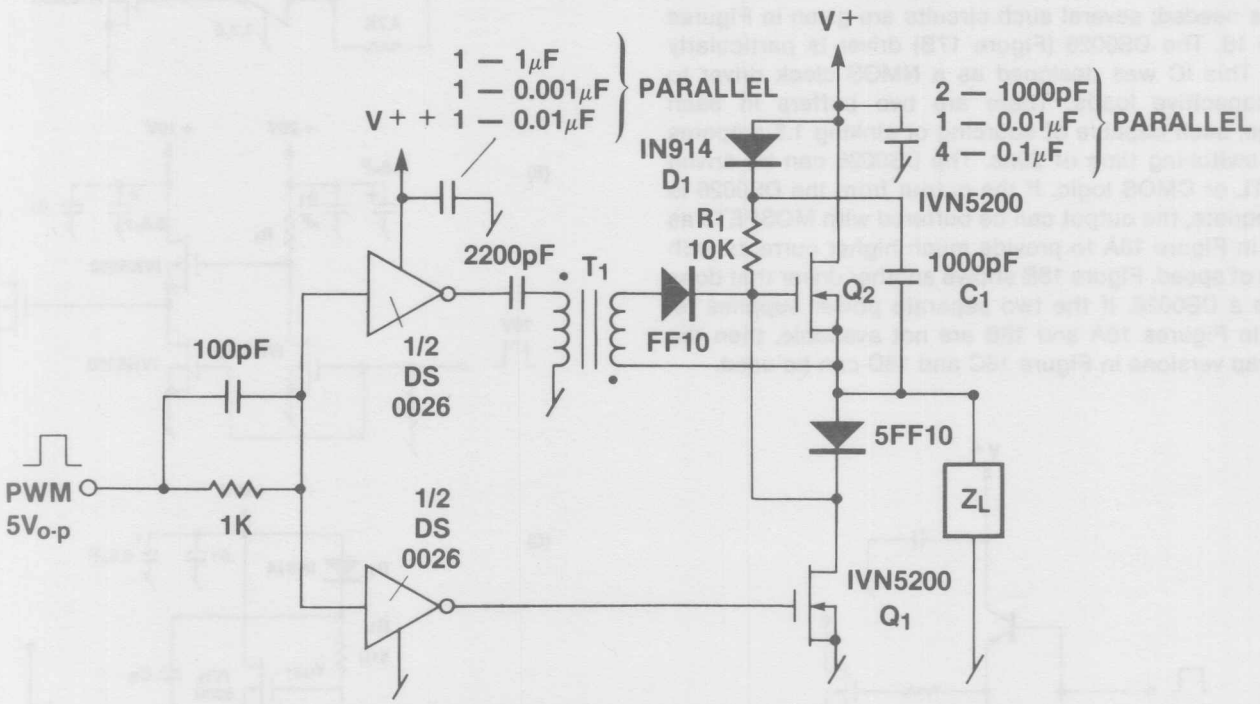


Figure 18. Bi-Directional Gate Drive Circuits

In applications which use a very large MOSFET or a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge quickly. Figure 19 shows a circuit which works very well with large-capacitance loads. When the input to the driver is zero, Q_1 is held in conduction by ½ of the DS0026. Q_2 is clamped off by Q_1. When a positive input occurs, Q_1 is turned off and a current pulse is applied to the gate of Q_2 by the other half of the DS0026 through T_1. After about 20ns, T_1 saturates and Q_2 is held on by its own C_{gs} and the bootstrap circuit made up of C_1, D_1 and R_1. For pulses less than 50μs the bootstrap circuit may not be needed as the input capacitance of Q_2 discharges very slowly. At the end of the positive input pulse, Q_1 turns on shutting off Q_2.



T_1 — is three turns 30 bifilar on a ferrite bead.

PERFORMANCE SUMMARY

Z_L	V+	V++	ns			
			t_{dr}	t_r	t_{df}	t_f
5Ω & 1000pF	20	15	22.5	7	15	7
4700pF	20	15	22.5	15	16	15.5
5Ω	20	15	23	11	14	4.5
5Ω	50	20	22	18	14	4
100' RG223/U Terminated in 51Ω	20	15	20.5*	19	13*	6.5

*Measured at input to cable.

Figure 19. Very High Speed Driver

The power driver circuit in Figure 19 can be modified to provide a direct coupled drive for a buck regulator as shown in Figure 20. Again the bootstrap portion of the circuit may not be needed when the switching frequency is above 10kHz.

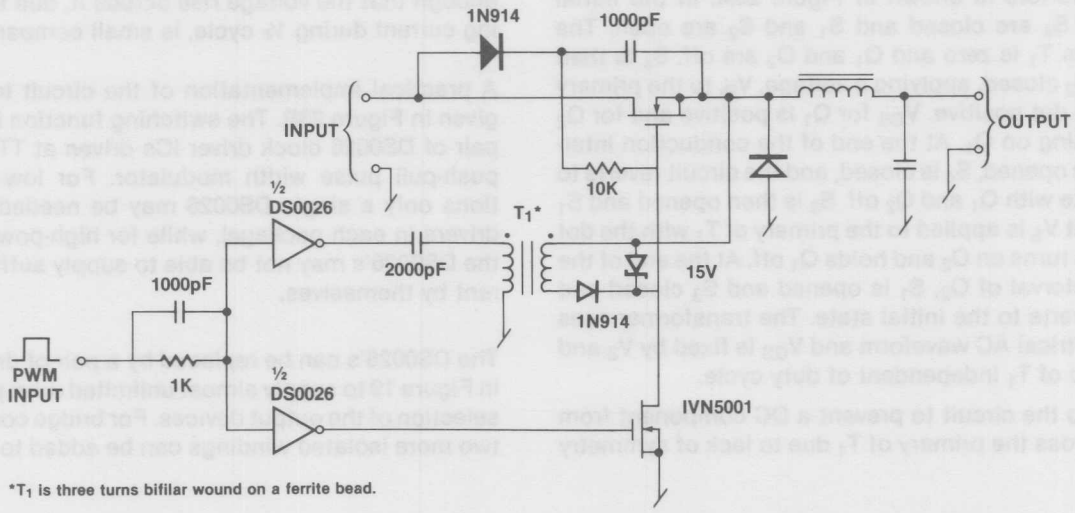


Figure 20. Gate Drive Scheme for MOSFET Buck Regulator

It is possible to use inductive energy storage schemes to drive MOSFETs; two possibilities are given in Figure 21. Energy is stored in L_1 during the OFF time of Q_2 and then discharged into the gate of Q_2 during conduction. The major disadvantage of these drive schemes is that the discharge current through the zener clamps must be maintained during the entire ON time of Q_2. This may greatly increase the drive power required.

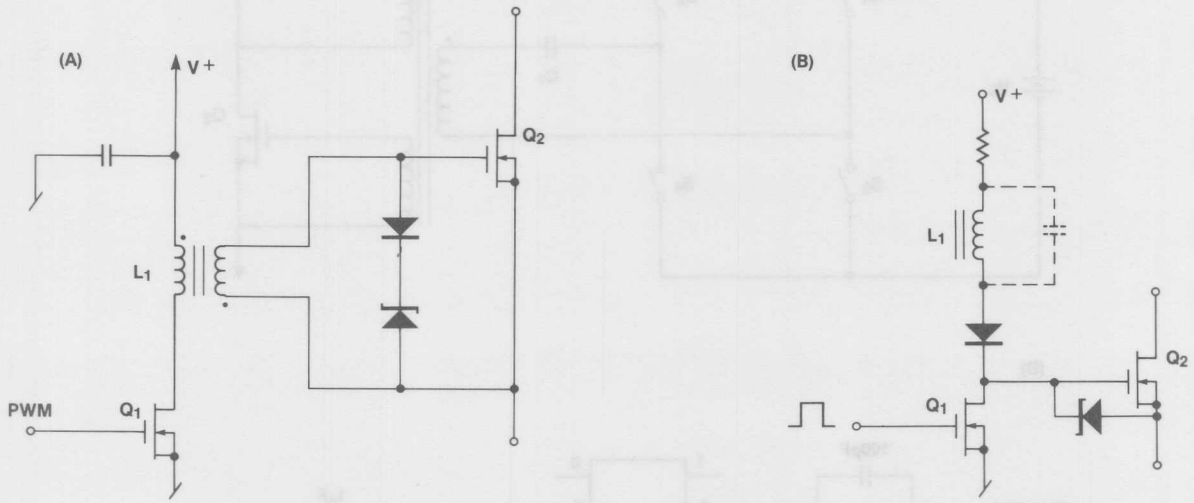


Figure 21. MOSFET Drive Circuits Using Stored Energy

Many applications require transformer isolation between the switches and the driver circuitry; Figure 22A shows a very simple means to accomplish this. Unfortunately this simple circuit has a major problem. As shown in Figure 22B, the transformer winding volt-seconds product must average zero. This means that the gate enhancement voltage will vary with duty cycle, being greater at low duty cycles. If a wide range of duty cycles must be accommodated the switch will be over-driven at low duty cycles and under-driven at high duty cycles. As was shown earlier, this can lead to large variations in the total switching time. However, for those applications where only a moderate variation in duty cycle is required this simple circuit can work very well.

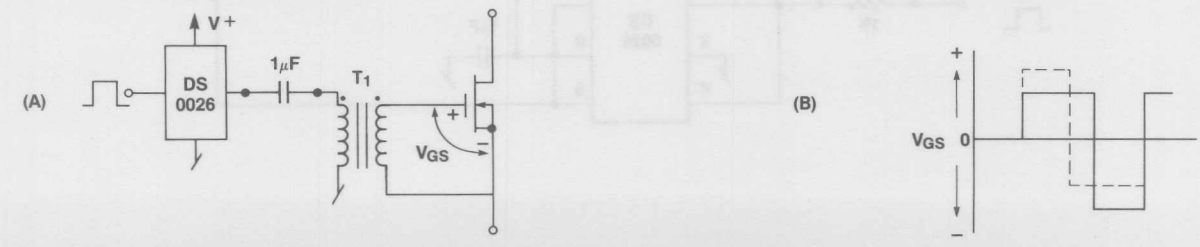


Figure 22. Transformer Coupled MOSFET Drive Ciruit

There are transformer-coupled drive circuits where V_{GS} does not vary with duty cycle. A circuit that can be used in symmetrical converters is shown in Figure 23A. In the initial state S_3 and S_4 are closed and S_1 and S_2 are open. The voltage across T_1 is zero and Q_1 and Q_2 are off. S_4 is then opened and S_2 closed, applying a voltage, V_S, to the primary of T_1 with the dot positive. V_{GS} for Q_1 is positive and for Q_2 negative, turning on Q_1. At the end of the conduction interval of Q_1, S_2 is opened, S_4 is closed, and the circuit reverts to the initial state with Q_1 and Q_2 off. S_3 is then opened and S_1 closed, so that V_S is applied to the primary of T_1 with the dot negative. This turns on Q_2 and holds Q_1 off. At the end of the conduction interval of Q_2, S_1 is opened and S_3 closed and the circuit reverts to the initial state. The transformer sees only a symmetrical AC waveform and V_{GS} is fixed by V_S and the turns ratio of T_1 independent of duty cycle.

C_1 is added to the circuit to prevent a DC component from appearing across the primary of T_1 due to lack of symmetry in the drive switching times. The value of C_1 is determined by the magnetizing current of T_1. C_1 should be large enough that the voltage rise across it, due to the magnetizing current during ½ cycle, is small compared to V_S.

A practical implementation of the circuit in Figure 23A is given in Figure 23B. The switching function is provided by a pair of DS0026 clock driver ICs driven at TTL levels from a push-pull pulse width modulator. For low-power applications only a single DS0026 may be needed (there are two drivers in each package), while for high-power applications the DS0026's may not be able to supply sufficient drive current by themselves.

The DS0026's can be replaced by a pair of drivers like those in Figure 19 to supply almost unlimited drive power by proper selection of the output devices. For bridge converter circuits, two more isolated windings can be added to T_1.

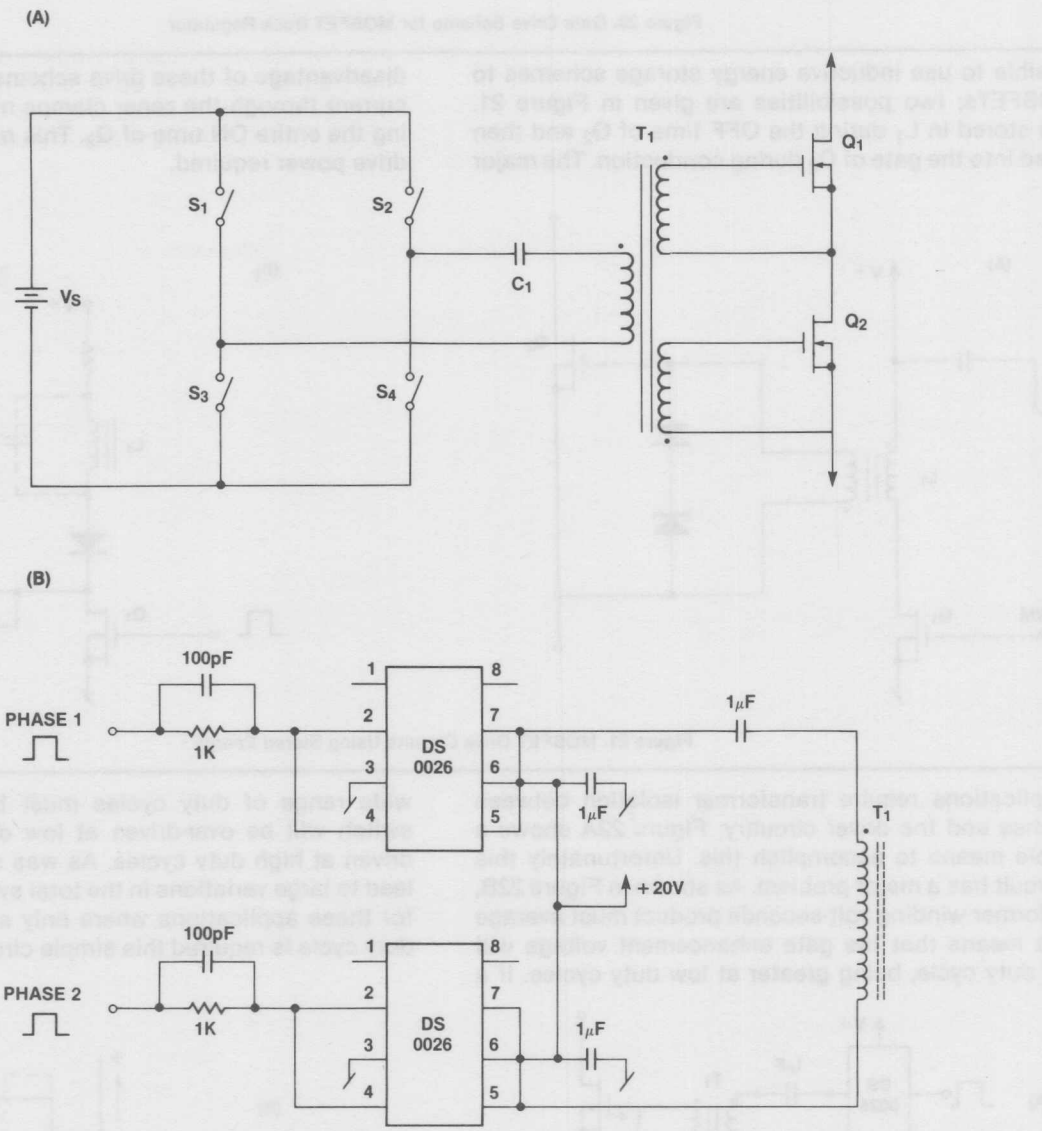
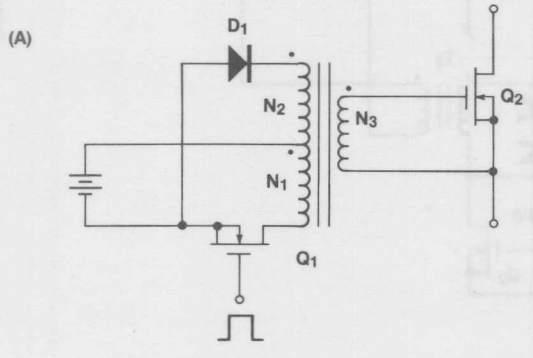


Figure 23. Symmetrical Transformer Coupled Drive Circuit

Figure 24A shows a transformer coupled circuit that will provide constant V_{GS} in asymmetrical converters. This circuit is a variation of the feed-forward converter. At the beginning of the positive input pulse, Q_1 turns on driving Q_2 into conduction. At the end of the input pulse, Q_1 turns off. The voltages across the transformer windings reverse, shutting off Q_2, and the energy stored in the core is discharged through D_1 into the source. While very simple, the circuit has two drawbacks. First, the energy stored in the core is a function of the duty cycle. The turn-off current for Q_2 is the magnetizing current for T_1, which is a function of duty cycle. The second problem occurs if the current in D_1 goes to zero during the off time of Q_2. This leaves the gate connected to winding N_3, which may well have sufficient impedance to cause dV_{DS}/dt triggering problems. By adding Q_3[3], as shown in Figure 24B, from gate to source of Q_2, these problems can be overcome. At turn-off, Q_3 is driven on by the energy in T_1 clamping the gate of Q_2. Even after all the energy in T_1 is discharged, Q_3 still presents a relatively low impedance at the gate of Q_2.



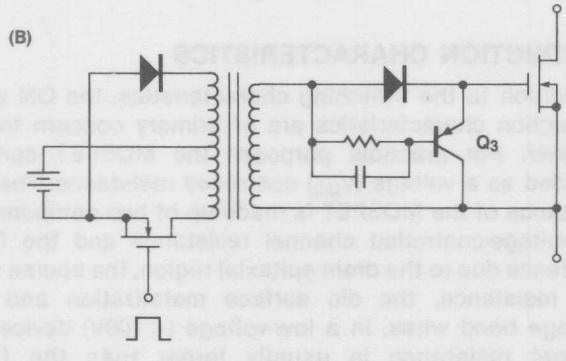


Figure 24

There are many other possible variations of both primary and secondary arrangements, and a few of these are summarized in Figure 25.

There is a basic limitation to the maximum duty cycle of single-transformer drive circuits. Over the period of one cycle the winding volt-second product must average zero. During the switch ON time the winding voltage is determined by the required enhancement voltage, V_{GS}. During the OFF time V_{GS} is limited by the breakdown voltage, BV_{GS}, of the gate. The maximum duty cycle is:

$$D_{MAX} = \frac{BV_{GS}}{BV_{GS} + V_{GS}} \quad (8)$$

Exactly the same problem exists in a bipolar junction transistor. However, when using a BJT, it is possible to use a diode in series with the emitter to arbitrarily increase BV_{BER} at the expense of increased voltage drop during conduction. This trick does not work with MOSFETs, since the leakage current of the diode will be much larger than the leakage of the MOSFET gate and all the reverse voltage still appears across the gate.

Another disadvantage of single-transformer circuits is that the transformer must be able to support V_{GS} during the entire ON time of the switch. Given the typical enhancement voltage of 10 to 20 volts this makes the transformer relatively large.

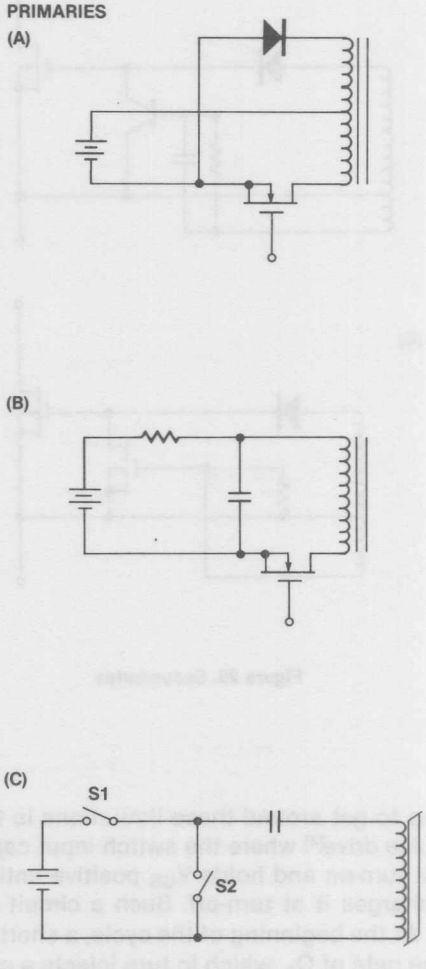


Figure 25. Primaries
Secondaries on next page

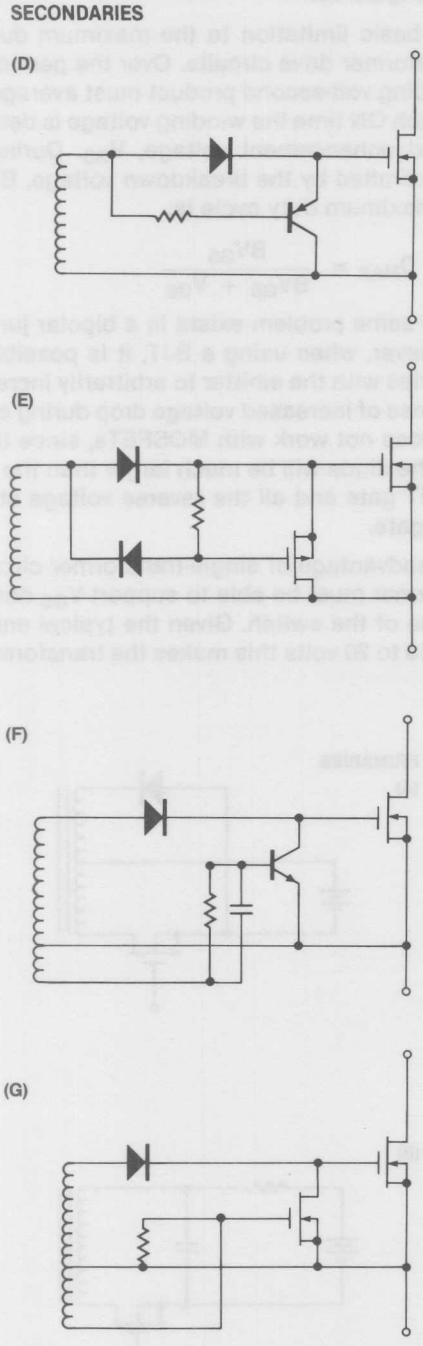


Figure 25. Secondaries

One means to get around these limitations is to use some form of pulse drive[4] where the switch input capacitance is charged at turn-on and holds V_{GS} positive until a negative pulse discharges it at turn-off. Such a circuit is shown in Figure 26. At the beginning of the cycle, a short pulse is applied to the gate of Q_1, which in turn injects a current pulse into the gate of Q_4 turning it on. Q_4 remains on due to the stored charge in the gate until a turn-off pulse is applied to Q_2. This turns on Q_3, which discharges the gate of Q_4 and turns it off. Despite the relative complexity, the circuit has several advantages. T_1 and T_2 can be designed to have very low leakage inductance, which makes fast transitions in Q_4 possible. There is no inherent limitation on duty cycle, and Q_4 may be kept on continuously by periodically pulsing Q_1 to replenish the charge in the gate of Q_4. The main disadvantage of this circuit, other than its complexity, is the high gate impedance during the off period, determined by R_1. To prevent V_{GS} from sagging significantly during the ON period, R_1 must be relatively large. If this drive scheme is used in a circuit that subjects Q_4 to a positive drain-source voltage transition during the off period, Q_4 may be triggered into conduction.

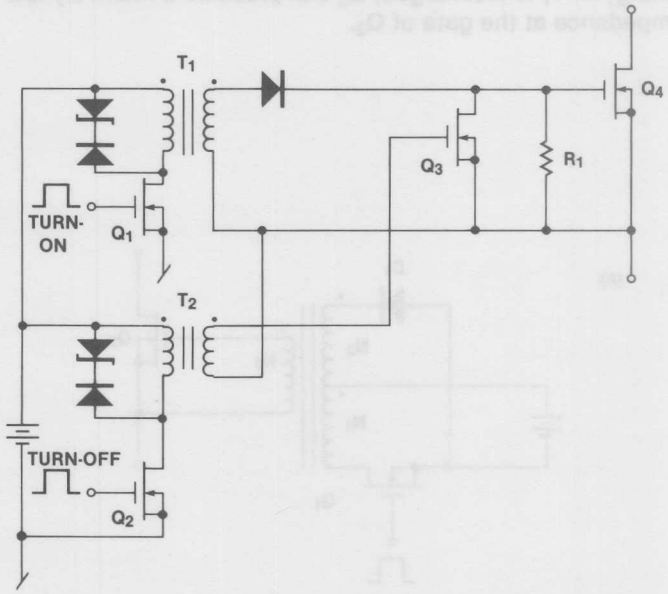


Figure 26. Pulsed Gate Drive Circuit

CONDUCTION CHARACTERISTICS

In addition to the switching characteristics, the ON state conduction characteristics are of primary concern to the designer. For practical purposes the MOSFET can be regarded as a voltage (V_{GS}) controlled resistance. The ON resistance of the MOSFET is made up of two components: the voltage-controlled channel resistance and the fixed resistance due to the drain epitaxial region, the source area bulk resistance, the die surface metalization and the package bond wires. In a low-voltage (<100V) device the channel resistance is usually larger than the fixed resistances. In a high-voltage device, however, the ON resistance is dominated by the resistance of the epitaxial drain region when the device is fully enhanced. Figure 27 shows the variation of $r_{DS(ON)}$ with V'_{GS} ($V'_{GS} = V_{GS} - V_{th}$) and I_D for a 450V two-ampere MOSFET (IVN6000 KNT). Note that $r_{DS(ON)}$ increases with I_D. The change in $r_{DS(ON)}$ is very abrupt as V_{GS} is increased.

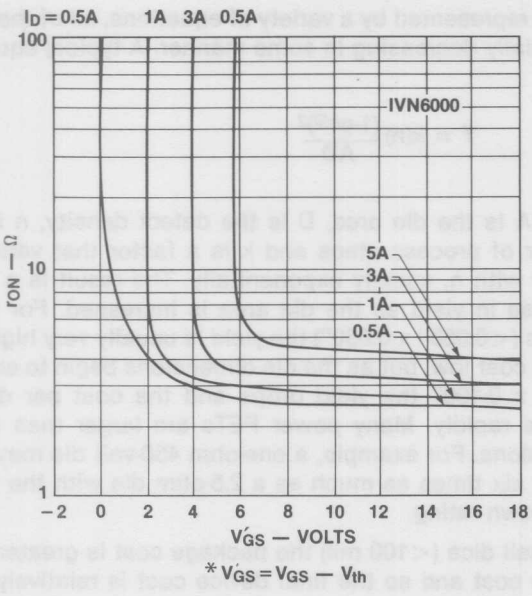


Figure 27. Variation of r_{ON} with V_{GS} and I_D

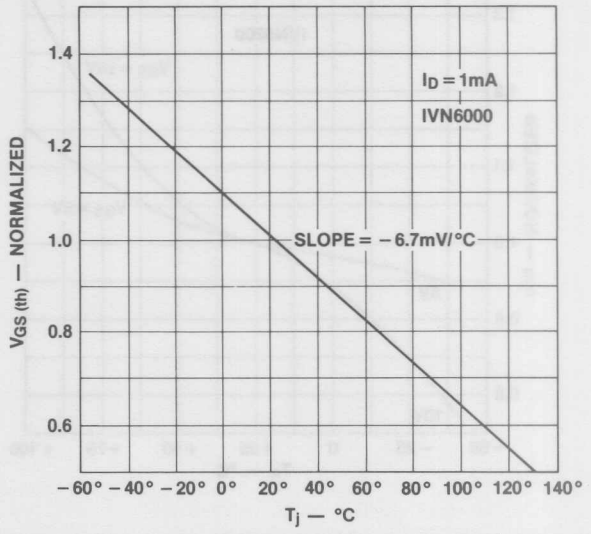


Figure 29. Variation of Threshold Voltage with Temperature

$r_{DS(ON)}$ is also a function of temperature, as shown in Figure 28. For $V_{GS} > 3$ volts, the normal region for power switch operation, the temperature coefficient is positive. This is one of the major advantages of the MOSFET over the bipolar, and accounts for the absence of lateral thermal instability induced second breakdown and the ease with which multiple devices may be paralleled. Below $V_{GS} = 3V$, $r_{DS(ON)}$ begins to display a negative temperature coefficient. This is due to the temperature coefficient of V_{th} as shown in Figure 29. For this particular device the temperature coefficient of V_{th} is about −6.7 mV/°C. For V_{GS} values near V_{th}, $r_{DS(ON)}$ is dominated by the channel resistance, which in turn is a strong function of V_{th}. For switching applications, this region is normally traversed very quickly during turn-on or turn-off and the negative temperature coefficient region is not a problem. Figures 30 and 31 show the normalized value of $r_{DS(ON)}$ as a function of temperature for a high-voltage (Figure 30) and a low-voltage (Figure 31) MOSFET. In the high-voltage device the temperature coefficient of $r_{DS(ON)}$ is 0.7 to 0.9%/°C. Because of the relatively greater contribution of the channel resistance to $r_{DS(ON)}$ in the low-voltage device, the variation of V_{th} with temperature reduces the temperature coefficient of $r_{DS(ON)}$ to 0.2 to 0.5%/°C. A very rapid means for determining the maximum value of I_D for a given V_{DS} and V_{GS} is to use the curves given in Figure 32.

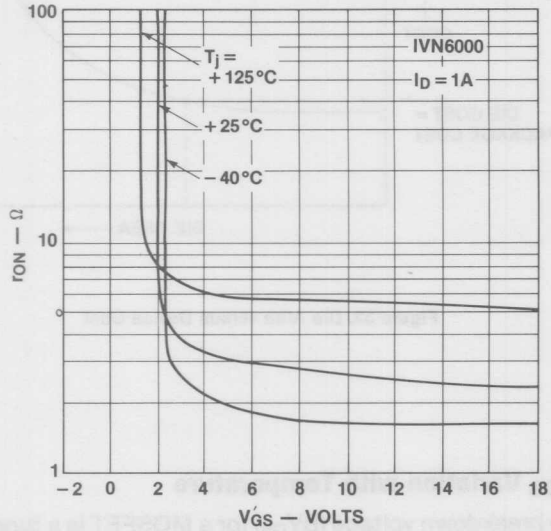


Figure 28. Variation of r_{ON} with Temperature

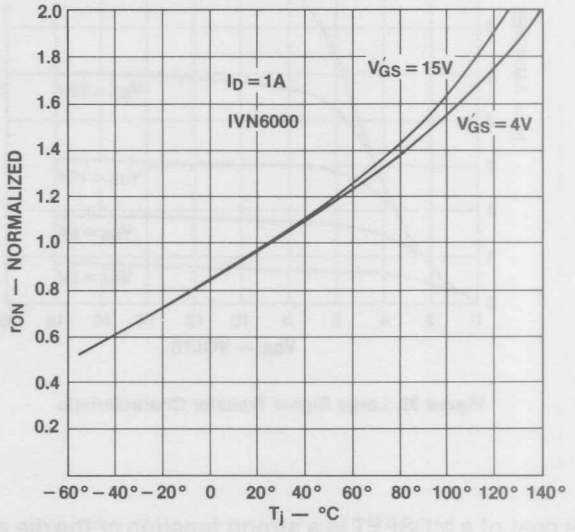


Figure 30. Variation of ON Resistance with Temperature for High-Voltage Power MOS

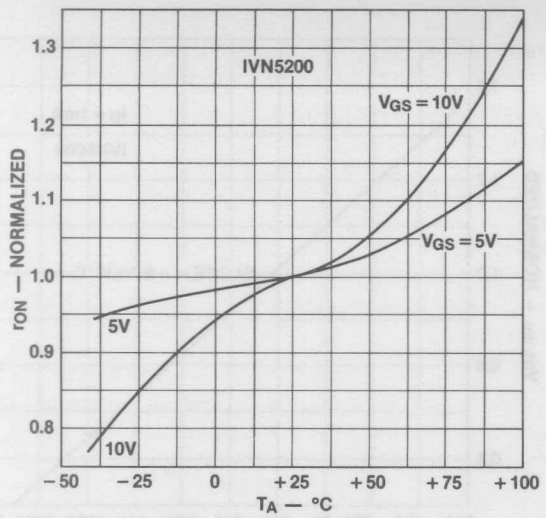


Figure 31. ON Resistance Variation with Temperature for Low-Voltage Power MOS

For a given structure and voltage rating, the ON resistance of a MOSFET is an inverse function of the die area. If half the ON resistance is desired the die area must be doubled.

For a given structure and die area, $r_{DS(ON)}$ increases very rapidly with breakdown voltage. The relationship is:

$$r_{DS(ON)} \propto BV_{DS}^{2.5\text{-}2.7} \quad (9)$$

The result is that a high-voltage, low-$r_{DS(ON)}$ device requires a large die.

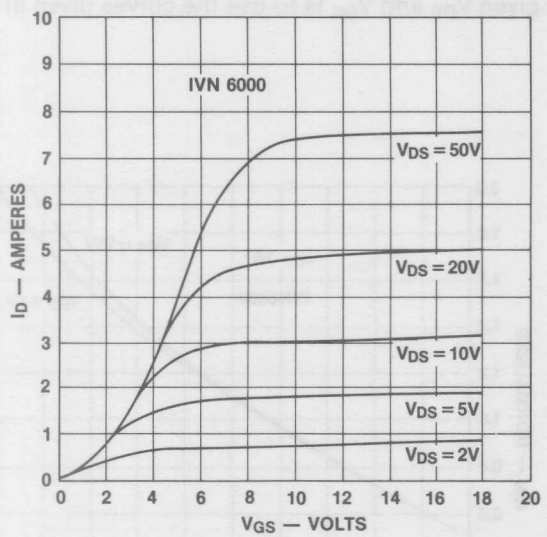


Figure 32. Large Signal Transfer Characteristic

The cost of a MOSFET is a strong function of the die area. If a large die area is used to reduce the ON resistance, the number of dice per wafer will decrease; additional dice are lost due to inherent wafer defects and the increased scrap zone around the wafer center and periphery. The yield (Y) can be represented by a variety of equations, all of them exponentially decreasing in some manner. A typical equation is:

$$Y = k(n)\frac{(1\text{-}e^{AD})^2}{AD} \quad (10)$$

where A is the die area, D is the defect density, n is the number of process steps and k is a factor that varies inversely with n, usually exponentially. The result is a rapid decrease in yield as the die area is increased. For small devices (<0.050" x 0.050") the yield is usually very high and the die cost low, but as the die dimensions begin to exceed 0.100" x 0.100" the yield drops and the cost per die increases rapidly. Many power FETs are larger than those dimensions. For example, a one-ohm 450-volt die may cost four to six times as much as a 2.5-ohm die with the same breakdown rating.

For small dice (<100 mil) the package cost is greater than the die cost and so the final device cost is relatively constant but as the die cost exceeds the package cost the total device cost becomes exponential with die area. This is shown qualitatively in Figure 33.

The $r_{DS(ON)}$ given in the data sheets is usually for a junction temperature of 25°C and the designer must calculate the actual value of $r_{DS(ON)}$ for the particular application. The actual $r_{DS(ON)}$ is:

$$r_{DS(ON)} = r_{DS(ON)}\left(1 + \frac{\alpha}{100}\right)^{T_j\text{-}25\,°C} \quad (11)$$

where $r_{DS(ON)}$ is the resistance for T_j = 25°C at the design I_D and V_{GS} and α is the averaged temperature coefficient of the ON resistance at the design T_j.

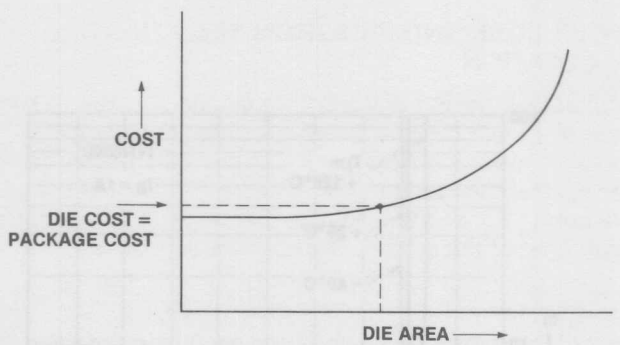


Figure 33. Die Area versus Device Cost

BV_{DS} Variation with Temperature

The breakdown voltage (BV_{DS}) for a MOSFET is a function of temperature as shown in Figure 34. At high temperatures BV_{DS} is above the data sheet values, but at low temperatures it can be significantly lower. For those applications where the switch is exposed to a low temperature soak and

then turned ON, this should be taken into account even though most devices supplied by the manufacturer will have breakdowns well above the data sheet values.

Note that the MOSFET is not unique in displaying a lower breakdown voltage at lower temperature. BJTs also show this effect.

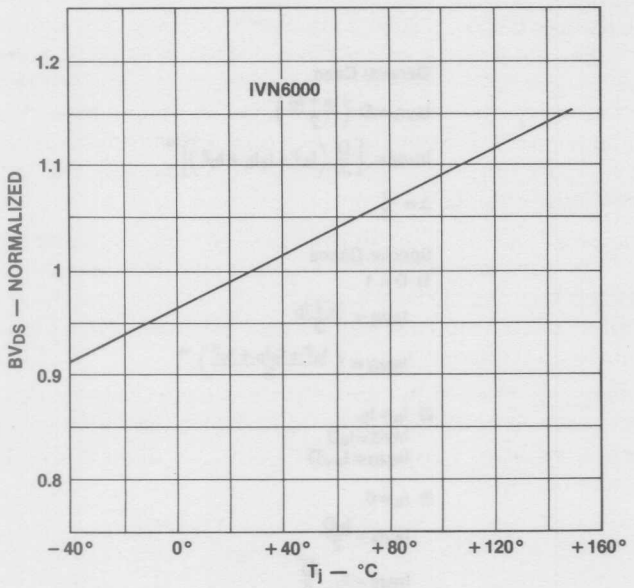


Figure 34. Breakdown Voltage Variation with Temperature

POWER LOSS AND JUNCTION TEMPERATURE CALCULATION

n a practical design situation the designer needs to know the total power dissipation and the junction temperature. The total power dissipation, P_d, is the sum of the switch loss, P_S, the conduction loss, P_C, some fraction of the gate drive power, P_G, and the leakage loss, P_L, due to I_{DSS} during the off time of the switch. The conduction loss is:

$$P_C = I^2_{D(RMS)}\, R_{ON} = I^2_{D(RMS)}\, r_{DS(ON)}\left(1 + \frac{\alpha}{100}\right)^{T_j\text{-}25\,°C} \quad (12)$$

The switching loss depends on the switching time and the nature of the drain load. The power loss due to a switching transition is:

$$P_S = f_S \int_0^{\tau} V_{DS}(t)\, I_D(t)\, dt \quad (13)$$

where f_S is the switching frequency and τ is the sum of the voltage and current transition times. Normally an exact solution is not required and the following approximations are usually adequate:

$$\text{for a resistive load, } P_S = \left(\frac{V_{DSMAX} \cdot I_{DMAX}}{6}\right) \tau f_S \quad (14)$$

$$\text{and for an inductive load, } P_S = \left(\frac{V_{DSMAX} \cdot I_{DMAX}}{2}\right) \tau f_S \quad (15)$$

A portion of the drive power, P_T, is dissipated in the internal gate resistance, R_G, and the remainder is dissipated in the drive circuit resistance, R_S. (If resonant charging is used most of the gate drive power may be recovered in the driver.) The gate dissipation, P_G, is:

$$P_G = P_T\left(\frac{R_G}{R_G + R_S}\right) \quad (16)$$

R_G is typically in the range of 1 to 10 ohm. Except in very high frequency switching applications (>100kHz) the drive power is insignificant compared to the other losses and is usually ignored.

Even when $V_{GS} = 0$, some current, I_{DSS}, will flow from drain to source. As shown in Figure 35, I_{DSS} is very small at room temperature but increases exponentially as the T_j is increased. The power loss due to leakage is:

$$P_L = V_{DS}\, I_{DSS}\,(1\text{-}D) \quad (17)$$

where V_{DS} is the drain source voltage during the OFF time, I_{DSS} is at the highest expected T_j, and D is the switch duty cycle. Since initially T_j is known only approximately, the value for P_L is only approximate. Normally, however, P_L is only a small part of the total loss so that the error is not usually significant.

In those applications where the MOSFET sees a substantially constant V_{DS} the power dissipation decreases with increasing T_j because of the positive temperature coefficient of $r_{DS(ON)}$, but this is not the typical switching application. More often the drain load is effectively a current source. In this mode of operation the power dissipation **increases** as T_j increases, providing a positive feedback mechanism that further increases T_j. Usually, however, for junction temperatures below 150°C, the gain coefficient of the positive feedback is less than one, so that a stable equilibrium point is reached. At higher temperatures (>150°C) it is possible to have no stable equilibrium point and the device can go into thermal runaway.

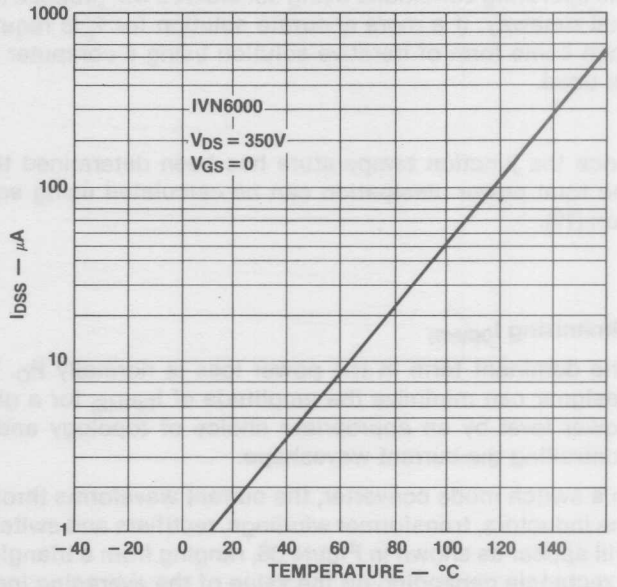


Figure 35. Drain-Source Leakage Current versus Temperature

To determine the junction temperature the following equations must be solved:

$$P_D = I^2_{D(RMS)}\, r_{DS(ON)} \left(1 + \frac{\alpha}{100}\right)^{T_j\text{-}25\,^\circ C} + P_S + P_L \quad (18)$$

$$T_j = T_A + R_{th(J\text{-}A)}\, P_D \quad (19)$$

Although equation (18) is transcendental and an exact analytical solution is not possible, a variety of solution methods are still possible. A most practical solution has been suggested by Gyma, Hyde and Schwartz[4] using a quadratic approximation for equation (12) which gives an answer accurate to a few percent. Equation (18) now takes the form:

$$P_D = I^2_{D(RMS)}\, r_{DS(ON)} (a_0 + a_1 T_j + a_2 T_j^2) + P_S + P_L \quad (20)$$

If equations (19) and (20) are combined:

$$A T_j^2 + B T_j + C = 0 \quad (21)$$

where:

$$A = a_2 R_{th(j\text{-}A)} I^2_{D(RMS)}\, r_{DS(ON)} \quad (22)$$

$$B = a_1 R_{th(j\text{-}A)} I^2_{D(RMS)}\, r_{DS(ON)} - 1 \quad (23)$$

$$C = T_A + R_{th(j\text{-}A)} (P_S + P_L) + a_0 R_{th(j\text{-}A)} I^2_{D(RMA)}\, r_{DS(ON)} \quad (24)$$

The following values for the coefficients a_0, a_1 and a_2 have been suggested:[4]

$$a_0 = 0.8650,\ a_1 = 4.443,\ \text{and}\ a_2 = 3.822 \times 10^{-5}$$

From equation (18):

$$T_j = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \quad (25)$$

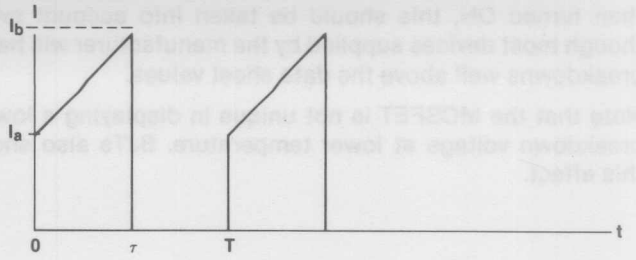
It has been shown[4] that the lesser of the two possible solutions is the correct choice. If the solution for T_j is complex the operating conditions being considered will produce thermal runaway. If a more accurate solution for T_j is required then some form of iterative solution using a computer can be used.

Once the junction temperature has been determined then the total power dissipation can be calculated using equation (19).

Minimizing $I_{D(RMS)}$

The dominant term in the power loss is normally P_C. The designer can minimize the amplitude of $I_{D(RMS)}$ for a given power level by an appropriate choice of topology and by controlling the current waveshape.

In a switch mode converter, the current waveforms through the inductors, transformer windings, rectifiers and switches will appear as shown in Figure 36, ranging from a triangle to a rectangle depending on the value of the averaging inductor and the load. For the capacitors, the waveforms will be similar, except that there will be no DC component (see Figure 37). The RMS and average values of the waveform are given in the figures.



General Case

$$I_{AVG} = D\left(\frac{I_a + I_b}{2}\right)$$

$$I_{RMS} = \left[\frac{D}{3}\left(I_a^2 + I_a I_b + I_b^2\right)\right]^{1/2}$$

$$\Delta = \frac{\tau}{T}$$

Special Cases

1) $D = 1$

$$I_{AVG} = \frac{I_a + I_b}{2}$$

$$I_{RMS} = \left(\frac{I_a^2 + I_a I_b + I_b^2}{3}\right)^{1/2}$$

2) $I_a = I_b$

$$I_{AVG} = I_a D$$

$$I_{RMS} = I_a\sqrt{D}$$

3) $I_a = 0$

$$I_{AVG} = \frac{I_b D}{2}$$

$$I_{RMS} = I_b\sqrt{\frac{D}{3}}$$

Figure 36. Average and RMS Values for Trapezoidal Waveforms

It can be shown that:

$$K \equiv \frac{I_a}{I_b} = f(L/L_C) \quad (26)$$

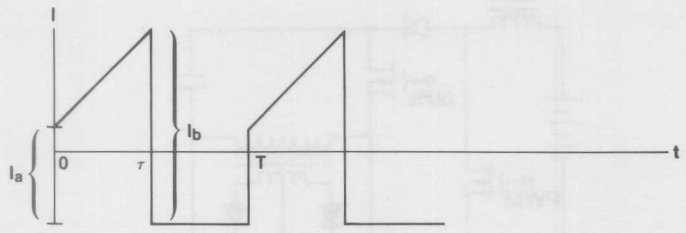
where, L = inductance of the averaging choke

L_C = is the critical inductance for a particular input voltage and load power

As L is increased, K goes from 0 (triangle) to 1 (rectangle). Substituting $K = I_a/I_b$ for the continuous choke current case:

$$I_{RMS} = \frac{I_{AVG}}{\sqrt{D}}\sqrt{\frac{K^2 + K + 1}{3\,(K+1)^2}} \quad (27)$$

For constant I_{AVG} and D, the normalized ($I_{RMS} = 1$ for $K = 1$) I_{RMS} is as shown in Figure 38. This curve shows the I^2R losses for triangular waveforms are 32% higher than for rectangular waveforms. It is also apparent that for $I_a/I_b > 0.6$, the additional losses incurred by having $L < \infty$ is only 2%, so from a practical point of view L need only be about twice L_C. Increasing the value of I_a/I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses usually dominate, increasing I_a/I_b reduces the switching loss also.



General Case

$$I_{RMS} = \left\{ D \left[\frac{I_a^2 + I_a I_b + I_b^2}{3} - \frac{D}{4}(I_a + I_b)^2 \right] \right\}^{1/2}$$

$$D = \frac{\tau}{T}$$

Special Cases

1) $D = 1$

$$I_{RMS} = \frac{I_b - I_a}{\sqrt{12}}$$

2) $I_a = I_b$

$$I_{RMS} = I_a\sqrt{D - D^2}$$

3) $I_a = 0$

$$I_{RMS} = I_b\sqrt{\frac{D}{3} - \frac{D^2}{4}}$$

Figure 37. RMS Value of AC Component of Trapezoidal Waveforms

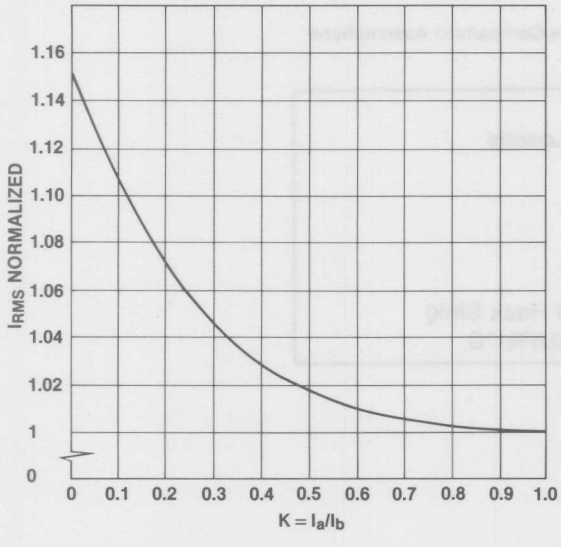


Figure 38. Variation of I_{RMS} with Trapezoidal Current Ratio

For the case of discontinuous inductor current ($L < L_C$), $I_a/I_b = 0$ and is no longer relevant since the waveforms are now triangular. For a given I_{AVG} the RMS current is:

$$I_{RMS} = \frac{I_{AVG}}{\sqrt{3D}} \tag{28}$$

A plot of equation (28) is given in Figure 39, where I_{AVG} is constant and I_{RMS} is normalized for $D = 1$. Obviously triangular current waveforms with high peak currents and low duty cycles are to be avoided if low losses are desired.

For the case where:

$I_a = I_b$:

$$I_{RMS} = \frac{I_{AVG}}{\sqrt{D}} \tag{29}$$

the curve in Figure 39 also applies.

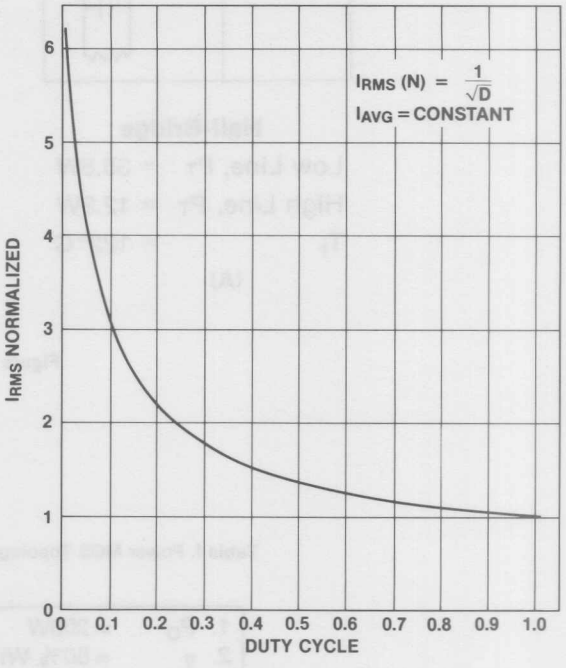
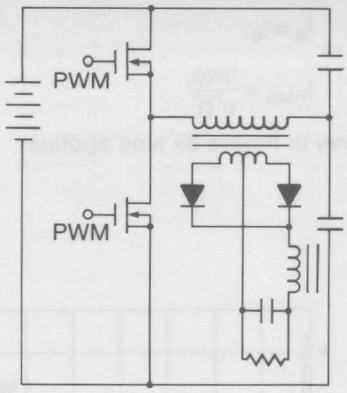


Figure 39. Variation of RMS Current with Duty Cycle for Triangular or Rectangular Current Waveforms

The topology selected can have a profound effect on the conduction losses. A simple example is shown in Figure 40. Figure 40A is a normal half-bridge quasi-squarewave converter, while 40B is an unmodulated half-bridge preceded by a boost regulator. Given the conditions in Table I, the power losses for (B) are much lower than (A). Because the cost of power MOSFETs is a strong function of $1/r_{DS}$, the three devices used in (B) may be much cheaper than the two devices in (A). While this is a fairly simple example, the boost derived family of converters generally provides lower MOSFET conduction losses than the buck derived converters. Figures 41A and 41B show two examples of boost derived converters, one using overlapping conduction and the other a secondary shunt switch. There are many other possible circuits that may be used. Unfortunately, the boost family of converters has disadvantages also:

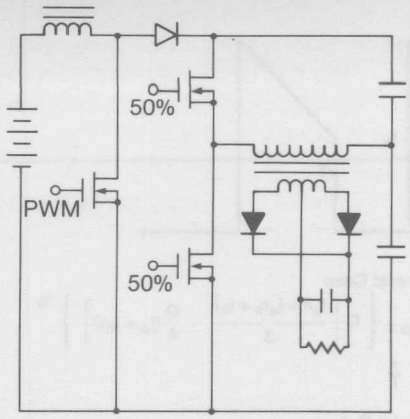
1. The control loop transfer function contains a right half-plane zero which is difficult to compensate for with single-loop feedback. By using multiple AC and DC loops, this problem can be overcome.
2. The output ripple current in a boost converter is discontinuous (the input current is continuous) so that the output ripple current is large.



Half-Bridge

Low Line, P_T = 35.8W
High Line, P_T = 12.9W
T_j = 122°C

(A)



Boost Regulator/Half-Bridge

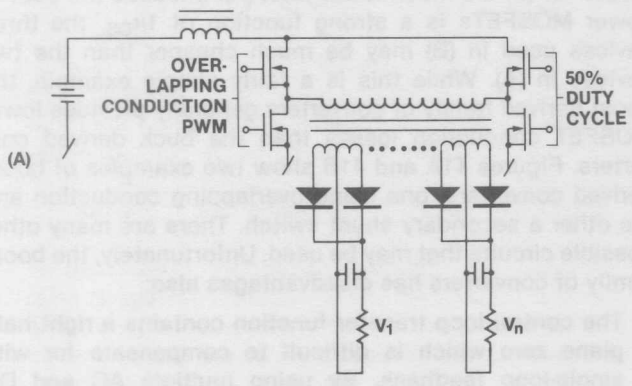
Low Line, P_T = 9.1W
High Line, P_T = 6.5W
T_j = 63°C

(B)

Figure 40. Topology Trade-Off

Table I. Power MOS Topology Conduction Loss Comparison Assumptions

1. P_O	= 200W
2. η	= 80% Without Switch Losses
3. V_{DC}	= 200V to 375V
4. T_A	= 50°C
5. r_{DS}	= 2.5Ω at 25°C
6. Filter Inductor is Large	
7. BV_{DSS}	= 450V to 500V
8. θJ_A	= 4°C/W (TO-3 Case and Heak Sink)
9. r_{DS} Temperature Coefficient is 0.6%/°C	



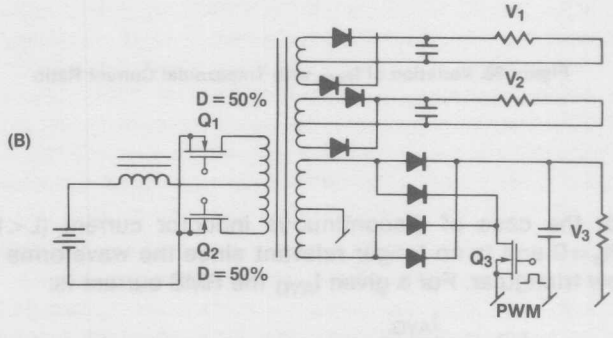


Figure 41. Boost Derived Power Converters

3. In those converters using overlapping conduction in the primary, a large voltage spike can be generated due to the interruption in the primary to secondary leakage inductance current. When the shunt switch is in the secondary, this spiking is greatly reduced.

Despite these drawbacks the significantly lower power losses of the boost family of converters make them very attractive for converters using MOSFET switches.

When compared to bipolar transistors, the MOSFET conduction losses for a given die area are always greater; the transistor's drive power and switching losses are greater than the MOSFET's. Figure 42 shows a comparison between transistors and MOSFETs of the total switch loss as a function of the switching frequency. The value of the crossover frequency, f_o, is a matter of some debate but lies in the region of 10 to 30kHz for devices of similar die area.

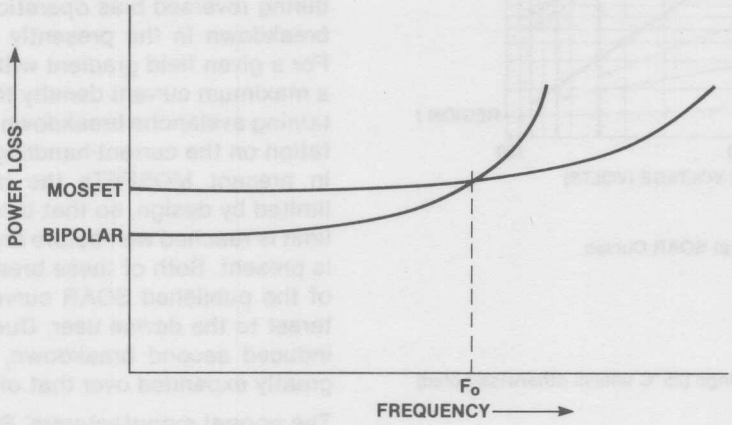


Figure 42. Comparison of BJT and MOSFET Losses
Note: F_o = 10 to 30kHz

SAFE OPERATING AREA

To achieve satisfactory service life from any power semiconductor, the circuit designer must assure that the device is operated within the voltage, current and thermal capabilities inherent in the particular device. To assist the designer, the manufacturer provides a table of maximum ratings, a safe operating area curve (SOAR) and a transient thermal impedance curve.

A typical absolute maximum ratings table is reproduced in Table II. While the information in the table is useful, it is not sufficient by itself for a power device. To adequately define safe operating conditions it is necessary to use the SOAR curve, like that reproduced in Figure 43. For a power MOSFET, the SOAR curve will have three boundary regions. Region I is defined by the breakdown voltage capability of the device. Region II is defined by the thermal capability of the device. Normally a maximum junction temperature of 150 °C is specified, so that in Region II the power dissipation is limited by a peak junction temperature of 150 °C. This results in Region II being defined by a family of curves that allows higher peak power for shorter pulse widths.

Region III is defined by the current capability of the device. The current capability of a given device may be limited by the bond wire diameter, the area of the bonding pad on the die, or by the metalization on the die surface. Whereas the breakdown voltage and junction temperature limitations can be readily determined by direct measurement, the current limitations are empirically derived from life testing. The maximum current is limited to a value which has been found to give an acceptable service life. In a bipolar transistor, the rapidly decreasing h_{FE} at high currents effectively discourages operation in excess of the current ratings. In a MOSFET, however, the gain is not reduced at high currents, and there may be a temptation, in fast pulse applications where a high drain-source voltage drop may be acceptable, to operate with very short high current pulses in excess of the ratings. Even if the device dissipation is very low, this is inadvisable for two reasons. First, the reliabilty or service life of the device is undefined and likely to be shortened, and second, if the current density in the device is increased sufficiently, it is possible to reach the level where current injected avalanche breakdown occurs, possibly destroying the device.

For a bipolar transistor the SOAR curves will have a fourth boundary. This region is defined by the thermally-induced second breakdown characteristic. In a bipolar device there are several ways to induce secondary breakdown. The first is thermal, where the negative temperature coefficient of V_{BE} causes localized hot spots to be formed. When the temperature of a hot spot is sufficiently high, its impedance is drastically reduced, funneling the collector current through a small area, usually destroying the device. Another mechanism for inducing secondary breakdown is via avalanche breakdown. If the collector voltage is raised to the breakdown point of the collector-base junction and a significant current allowed to flow, the device will go into secondary breakdown. It has been widely advertised that MOSFETs do not exhibit secondary breakdown. This is not true. It is generally accepted that at normal junction temperatures, the thermally-induced secondary breakdown phenomenon so prevalent in bipolar devices is not present in

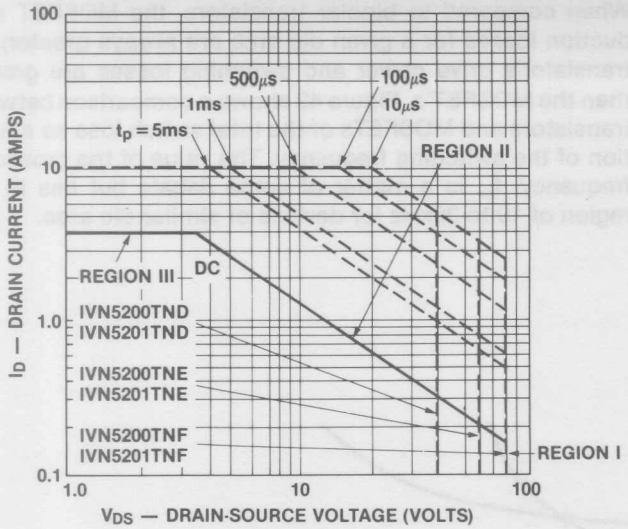


Figure 43. Typical SOAR Curves

Table II. Absolute Maximum Ratings (25 °C unless otherwise noted)

Drain-source Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Drain-gate Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Continuous Drain Current (see note 1)	4.0A
Peak Drain Current (see note 2)	10A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	10 °C/W
Continuous Device Dissipation at (or below)	
25 °C Case Temperature	12.5W
Linear Derating Factor	100mW/ °C
Operating Junction	
Temperature Range	−55 °C to +150 °C
Storage Temperature Range	−55 °C to +150 °C
Lead Temperature	
(1/16 in. from case for 10 sec.)	+300 °C

Note 1. T_C = 25 °C; controlled by typical $R_{DS(ON)}$ and maximum power dissipation.

Note 2. Pulse width 80μs, duty cycle 1.0%.

MOSFETs; the avalanche-induced secondary breakdown, however, is. This is not surprising; as shown in the earlier discussion, the MOSFET structure has within it an NPN transistor, and the voltage limit on the device is the base-collector junction breakdown voltage. The breakdown voltage is equivalent to BV_{CEX} in a bipolar.

The current level at which primary breakdown becomes secondary breakdown is a function of the base emitter resistance, the temperature and the h_{FE} of the bipolar device. In a MOSFET, the base and emitter are shorted right on the die, and for reasons of improving the dV_{DS}/dt characteristic, the resistance is made as low as possible. In addition, the h_{FE} of the MOSFET parasitic bipolar is much lower than a typical bipolar device. The result is that the current level at which primary breakdown becomes secondary breakdown is much higher in a MOSFET than it is in a comparable bipolar transistor. The device ratings are selected so that the maximum V_{DS} is well below the actual breakdown point in production devices.

Current-injected avalanche breakdown, present in bipolars during reversed bias operation, can also lead to secondary breakdown in the presently available types of MOSFETs. For a given field gradient within the semiconductor there is a maximum current density threshold above which self-sustaining avalanche breakdown can occur. This is a basic limitation on the current-handling capability of a power device. In present MOSFETs the internal current densities are limited by design, so that the junction temperature thermal limit is reached well before any current-injected avalanching is present. Both of these breakdown modes lie well outside of the published SOAR curves and neither is of direct interest to the device user. Due to the absence of thermally-induced second breakdown, the SOAR for a MOSFET is greatly expanded over that of a comparable bipolar.

The normal manufacturers' SOAR curve is given for a case temperature of 25 °C and either DC or a single pulse. In the real world of case temperatures above 25 °C and repetitive pulses, the designer must modify the standard SOAR curves for his particular application. This can be done by using the transient thermal impedance $Z_{(th)}$ curves which are generally made available by the manufacturer.[7]

dV/dt LIMITATIONS AND MOSFET POWER SWITCHES

Most designers are well aware of the dV/dt limitations of SCRs which, if exceeded, can cause these devices to turn on in the absence of a normal trigger pulse. However, it is not generally appreciated that a similar, and in some cases equally detrimental, phenomenon can appear in both bipolar transistors and MOSFET power switches.

Waveforms Responsible for Spurious Turn-On

Turn-on due to dV/dt can occur in any power circuit that subjects the power switch to a positive dV/dt during the normal operating cycle. A very common circuit application where this occurs regularly is the pulse width modulated switching regulator. An example of a half-bridge circuit is shown in Figure 44 along with the collector (or drain) voltage and current waveforms in Figure 45. The normal operating conditions are shown in Figure 45A. Q_1 turns on at t_0 and off at t_1. Q_2 turns on at t_2 and off at t_3 where a negative current spike flows through Q_1 and D_1 due to the transformer leakage inductance. Normally most, but not all, of the reverse current at t_3 will flow through D_1. From Figure 45A it is evident that

Q_1 is subjected to a positive dV/dt during the operating cycle when the switch is in one of two states: at t_1, Q_1 has been conducting in the forward direction and at t_2, Q_1 is quiescent.

In some applications, such as resonant inverters, motor drivers or synthesized sine wave inverters, waveforms similar to those in Figure 45B can occur. The significant feature of this mode of operation is the **reverse** conduction of Q_1 and D_1 just prior to the application of a positive dV/dt on the collector. This is a third state in which the device may see a positive collector transition. Any or all of these states can occur in a very wide variety of power switching applications.

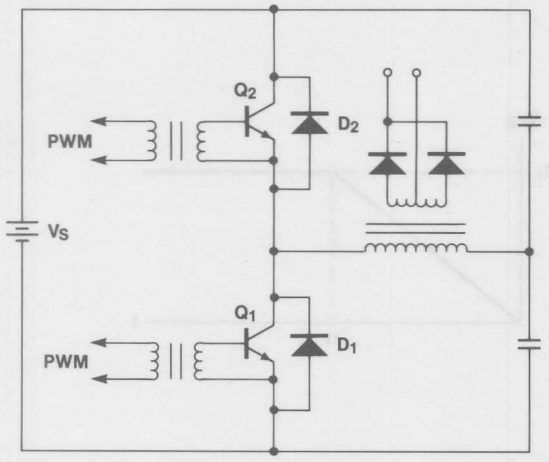


Figure 44. Typical Switching Regulator Circuit

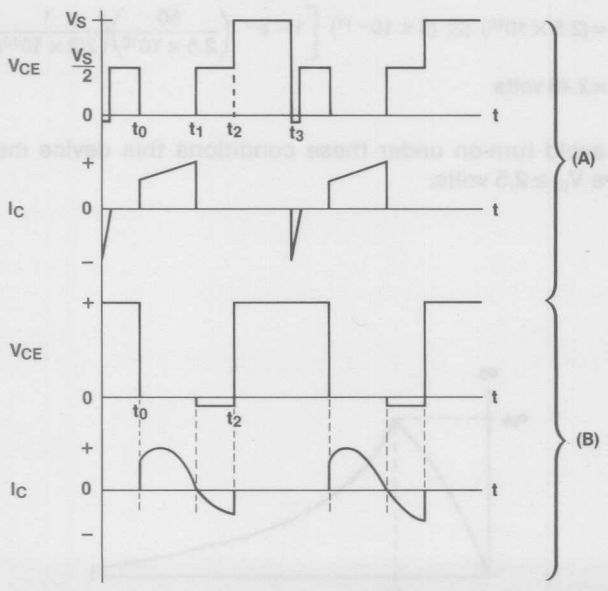


Figure 45. Q_1 Voltage and Current Waveforms

Mechanisms Responsible for Spurious Turn-On

Figure 46 shows equivalent circuits in which the effect of C_{ob}, C_{ie} and R_{BE} for the transistor and C_{gd}, C_{gs} and R_{gs} for the MOSFET are taken into account and separated from the basic device.

If a positive voltage ramp, V_{DS}, is applied to the drain of the MOSFET a current, I_1, will flow through the C_{gd}, C_{gs} and R_{gs} resulting in a positive value of V_{gs}. If I_1 is large enough V_{gs} will exceed the threshold voltage, V_{th}, of the MOSFET and it will turn on until V_{gs} drops below V_{th}. An identical effect is present in the bipolar device which will turn on if V_{BE} exceeds 0.6 to 0.7 volts.

The amplitude of I_1 is determined by the values for the capacitors, input resistances, E_1 and t_1.

The values for the capacitors depend on the type of device (bipolar or MOSFET), the design of the device, V_{DS} **and** the state of conduction immediately prior to the application of the ramp. The input resistances (R_{gs} and R_{BE}) are in part inherent in the devices and partly determined by the external circuit impedance. The threshold voltages (V_{th} or V_{BE}) are temperature variable and in the case of the MOSFET, V_{th} is a device design variable. Transistor h_{FE} also varies with temperture. E_1 and t_1 are of course determined by the external circuit.

Despite this apparent complexity, analytical solutions for V_{gs} or V_{BE} during the ramp can be derived which are of practical use.

General Model

For the purposes of calculating the voltage at the gate or base, the equivalent circuit shown in Figure 47 can be used with the appropriate component values. The ramp function is provided by the combination of a positive unit ramp starting at $t = 0$ and a negative unit ramp at $t = t_1$. The slope of the ramp, dV/dt, is:

$$\frac{dV}{dt} = \frac{E_i}{t_1} \tag{30}$$

The output voltage, $E_O(S)$, can be shown to be:

$$E_O(S) = \left(\frac{E_i}{t_1}\right)\left(\frac{C_1}{C_1 + C_2}\right)\left\{\left[\frac{1}{S(S + 1/R\,(C_1 + C_2))}\right] - \left[\frac{e^{-t_1 S}}{S(S + 1/R\,(C_1 + C_2))}\right]\right\} \tag{31}$$

By applying the following inverse Laplace transformations to equation 31:

$$\frac{1}{S(S + \alpha))} \xrightarrow{\pounds^{-1}} \frac{1}{\alpha}(1 - e^{-\alpha t}) \tag{32}$$

$$F(S)e^{-t_1 S} \xrightarrow{\pounds^{-1}} F(t\text{-}t_1) \tag{33}$$

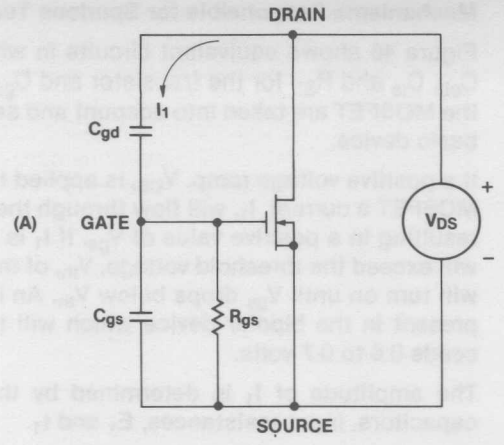
The time domain response for $e_O(t)$ can be obtained as:

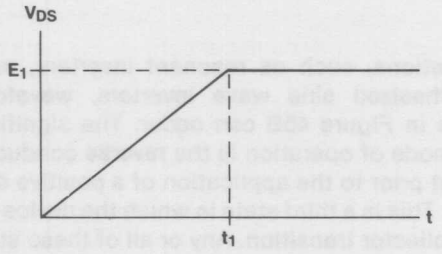
for $t \leq t_1$

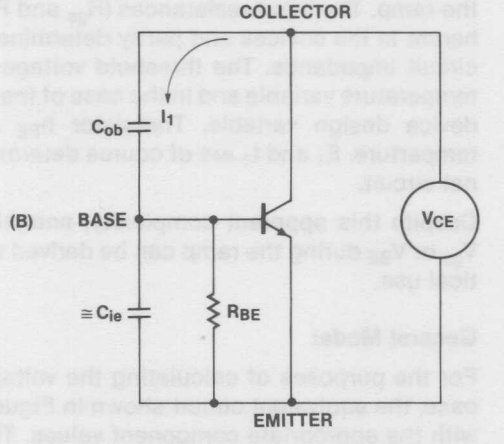
$$e_O(t) = \left(\frac{E_i\, R\, C_1}{t_1}\right)\left[1\text{-}e^{-t/R(C_1 + C_2)}\right] \tag{34}$$

and for $t \geq t_1$

$$e_O(t) = \left(\frac{E_1}{t_1}\right)(R\,C_1)\left(e^{-t/R(C_1 + C_2)}\right)\left(e^{t_1/R(C_1 + C_2)}\right) \tag{35}$$







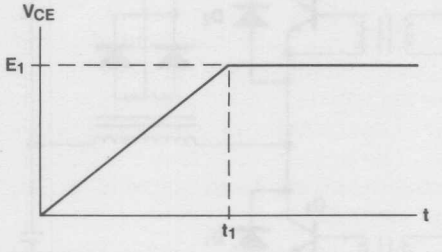


Figure 46. MOSFET and BJT Equivalent Circuits

The waveform represented by equations (34) and (35) is shown in Figure 48. For practical purposes, the only feature of the waveform that is of interest is the peak value of e_O, e_{PK}. The designer needs to know if e_{PK} is sufficiently large to turn on his device. By combining equations (30) and (34) and setting $t = t_1$, the expression for e_{PK} becomes:

$$e_{PK} = \left(\frac{dV}{dt}\right)(\tau_1)\left[1 - e^{-}\left(\frac{E_i}{dV/dt}\right)\left(\frac{1}{\tau_2}\right)\right] \quad (36)$$

where: $\tau_1 = R\,C_1$ (37)

$\tau_2 = R(C_1 + C_2)$ (38)

Example

For a MOSFET where $C_1 = 50pF$, $C_2 = 150pF$, $V_{DS} = 50V$, $dV/dt = 25V/ns$ and $R = 1\Omega$:

$$e_{PK} = (2.5 \times 10^{10})\ (2)\ (5 \times 10^{-11})\left[1 - e^{-}\left(\frac{50}{2.5 \times 10^{10}}\right)\left(\frac{1}{2(2 \times 10^{10})}\right)\right]$$

$e_{PK} = 2.48$ volts

To avoid turn-on under these conditions this device must have $V_{th} \geq 2.5$ volts.

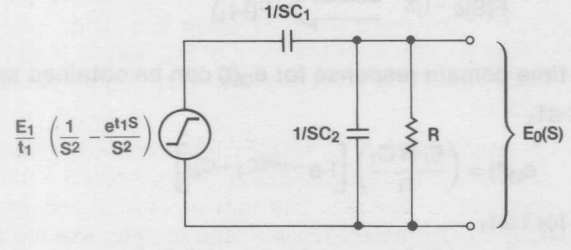


Figure 47. Equivalent Circuit

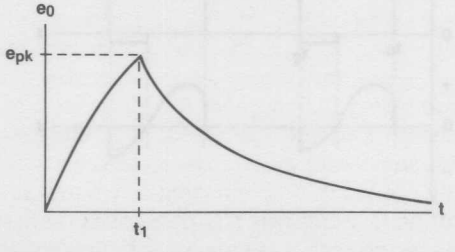


Figure 48. V_{GS} or V_{BE} Waveform

How to Determine the Appropriate Values for C_1 and C_2

As has been already mentioned, the values for C_1 and C_2 depend on the type of device selected and the design of the specific device. Once a specific device has been selected, the values for C_1 and C_2 will be dependent on the potentials applied to the device. The typical capacitance values for a high-voltage MOSFET were shown in Figure 5. While C_{gs} is relatively constant with variations in V_{DS}, C_{gd} is obviously not. It is possible to substitute the value of C_{gs} for C_2 and a relatively simple analytical expression for C_{gd}, for C_1 into equation (36) to determine e_{PK} but this would be somewhat clumsy. A simpler solution would be to determine an average value for C_1 from Figure 5 for the peak voltage the device will see.

A bipolar device in the quiescent state will display a capacitance characteristic very similar to that shown for the MOSFET. However, when either the base-emitter or base-collector junctions are forward-biased and conducting, the capacitance values are drastically changed. When the bipolar is conducting in the forward direction the base-emitter junction is forward-biased and displays a very large value of diffusion capacitance. This means that C_2 is large and the dV/dt capability is greatly **increased.** If on the other hand the device is conducting in the reverse direction then the collector base junction is forward-biased and C_1 is much larger. This greatly **decreases** the dV/dt capability of the device. Even if a diode is shunted across the bipolar (D_1 or D_2) some small current will still be available to forward bias the base-collector junction.

The three operating states defined earlier determine the choice of values for C_1 and C_2. Of the three conditions the reverse conduction mode is by far the worst and has the lowest dV/dt threshold. For the quiescent state for bipolars and MOSFETs, and the forward conducting state of the MOSFET, the amplitude of the current pulse due to dV/dt triggering is usually not damaging except in very fast circuits. In the forward conducting state in a bipolar, C_2 is so large that given the limits on bipolar switching speeds dV/dt triggering is not a problem. However, in the case where reverse conduction has occurred, the resulting pulse in a circuit like that in Figure 44 can destroy both devices. As a practical matter, it is difficult to measure the diffusion capacitances so the designer must test the desired device under actual circuit conductions for dV/dt capability.

The Parasitic Bipolar in MOSFETs

The present power MOSFET devices all have a parasitic bipolar transistor as an inherent part of the structure. The equivalent circuit for an N-channel device is given in Figure 49. For a P-channel device the parasitic transistor would be a PNP. The base and emitter connections of the parasitic transistor are connected together at the surface of the die to minimize the value of R_{BE} but there is still some resistance in the bulk of the semiconductor material. The value for R_{BE} will vary depending on the size of the die and the voltage rating but is generally 2Ω or less. In devices of similar design and voltage rating, C_{ob} increases with die size at the same rate as R_{BE} decreases so that τ_1 remains essentially constant. C_{ob} is essentially equal to C_{ds}. As the voltage rating is increased, C_{ob} decreases more rapidly than R_{BE} increases so that τ_1 is smaller in higher voltage versions of the same design.

The question when using a MOSFET is which device, the MOSFET or the parasitic bipolar, determines the dV/dt limit? Usually $C_{gs} < C_{ob}$, $R_g < R_{BE}$ and $V_{th} > V_{BE}$. As long as the user keeps the source impedance low during positive drain transitions the maximum dV/dt is determined by the bipolar. Too high a gate impedance can, however, lower the dV/dt rating by allowing the MOSFET to turn on.

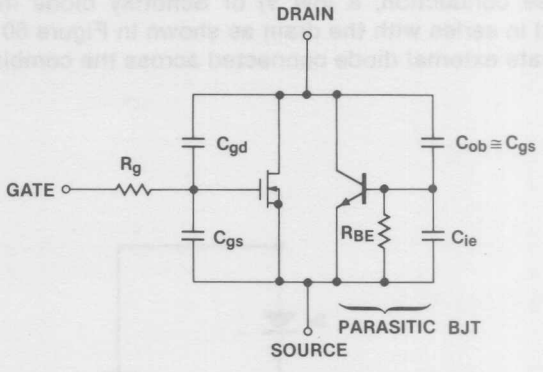


Figure 49. MOSFET Model Including Parasitic BJT

Another unpleasant possibility in a MOSFET is that if the parasitic NPN is turned on it may experience second breakdown due to thermal instability.

Temperature Effects

The threshold for dV/dt triggering will decrease with temperature for several reasons. V_{th} in a MOSFET has a negative temperature coefficient of about 6mV/°C. Similarly, V_{BE} in a bipolar has a negative temperature coefficient of about 2mV/°C. Typically for a bipolar $V_{BE} = 0.7$ and for a MOSFET $V_{th} = 2.0$ to 5.0V. The temperature coefficient for the bipolar is a larger percentage of the threshold voltage than in the MOSFET so that the degradation of dV/dt due to temperature-induced threshold shift is more pronounced in the bipolar.

The internal portion of R_g in the MOSFET is primarily due to the gate connection material. In some structures, particularly VMOS, the gate connections are made with aluminum which produces a very low R_g that does not vary greatly with temperature. DMOS devices on the other hand use poly silicon gate structures which have a higher R_g with a temperature coefficient of about 0.6 to 0.7%/°C. In the parasitic bipolar, R_{BE} will have a temperature coefficient of 0.6 to 0.7%/°C. In a bipolar switch most of R_{BE} will be in the external circuit and will probably not vary significantly with temperature.

The ON resistance of the MOSFET has a positive temperature coefficient while the bipolar has a negative temperature coefficient. The result is that at higher temperatures the MOSFET ON resistance will tend to decrease the amplitude of the current pulse due to dV/dt and the bipolar will tend to increase the current pulse.

The gain of the MOSFET is not greatly affected by temperature but the h_{FE} of both the parasitic transistor and the bipolar switch does increase with temperature. This means that if the bipolar is turned ON more current will flow at higher temperatures.

The duration of the current pulse caused by dV/dt triggering depends on the length of time e_O is above V_{th} and in the case of a transistor, the storage time is added to this. The storage time will increase with temperature.

If the dV/dt capability of the switch is not adequate due to reverse conduction, a low V_f or Schottky diode may be added in series with the drain as shown in Figure 50 and a separate external diode connected across the combination (D_2).

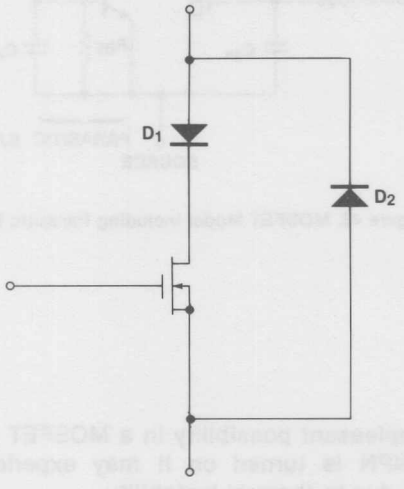


Figure 50. Method for Eliminating Reverse Conduction

USING THE INTERNAL DIODE

The parasitic transistor can be used as a rectifier or clamp diode in switching regulator circuits. For example (Figure 51), the clamp diode usually added in a bipolar bridge inverter comes for free in the MOSFET. The internal diode has the same breakdown voltage and current ratings as the MOSFET itself, because it uses the same silicon, metalization, bond wires and package. The reverse recovery time (t_{rr}) for the diode can be excellent. In the IVN5000 and 5200 series devices, $t_{rr} = 60$ns and in the IVN6000 $t_{rr} = 100$ns. There are several reasons for the high speed. First, the structure is an epitaxial diode with sharply-defined diffusions. Second, the doping of the p-region is done using an ion implant machine. The ion implant process produces dislocations in the crystal structure which can act as recombination centers to reduce the recovery time. Not all manufacturers use ion implant techniques, and there may well be a wide variation in t_{rr} for similar devices from different manufacturers or from the same manufacturer at different times when there has been a process change.

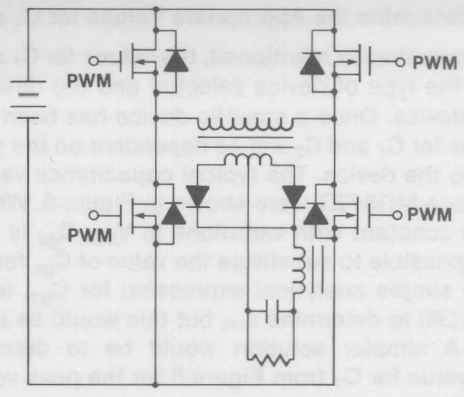


Figure 51. Quasi-Squarewave Bridge Converter

As shown in Figure 52, the forward voltage drop (V_f) characteristic is typical for a junction diode. Because of the large die areas normally used in a power MOSFET, V_f is quite low.

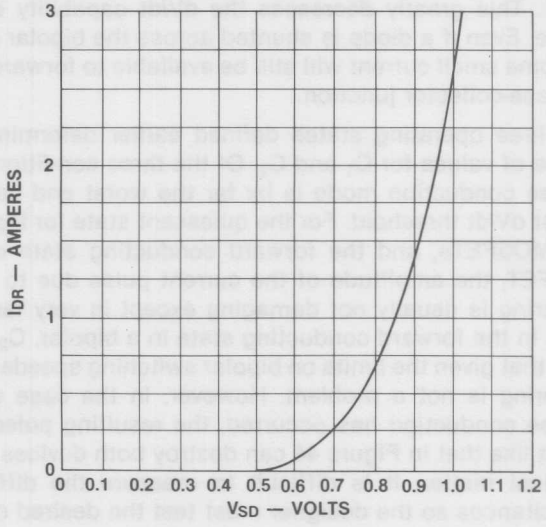
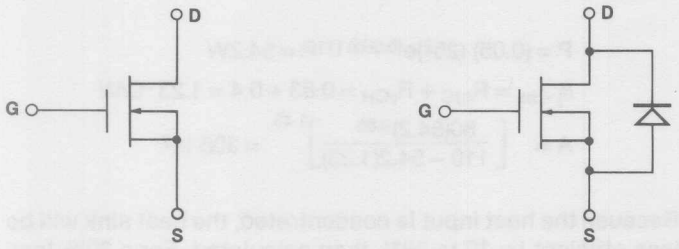


Figure 52. IVN6000 Diode Forward Voltage Characteristic

A MOSFET may be used as a bidirectional switch or as a synchronous rectifier. Referring to Figure 53, when the gate is made sufficiently positive with respect to the source, the MOSFET becomes essentially a resistor in which the current may flow in either direction, source to drain or drain to source. As long as the voltage drop across $r_{DS(ON)}$ is below 0.6 volts, the parasitic diode will not conduct appreciably and the FET can be used as a bidirectional power switch with zero offset voltage. If synchronous rectifier operation is desired, the gate-source voltage is zero when the drain-source voltage is positive, thereby blocking the flow of current. When the drain-source voltage reverses, the gate is driven positive and current flows from source to drain. The

user now has a majority carrier rectifier with no storage time and a switching time equal to that of the FET (usually a few ns). The voltage breakdown rating is, of course, equal to that of the FET. If the voltage drop across the FET exceeds the threshold of the parasitic diode, the current is bypassed around the FET and V_f assumes the characteristic of the diode.

The designer must keep in mind the dV/dt limitations of the internal diode.



(A) NORMAL SYMBOL FOR N-CHANNEL

(B) DIODE EMPHASIZED

Figure 53. Diode in MOSFET Structure

MULTIPLE DEVICE OPERATION

The positive temperature coefficient of $r_{DS(ON)}$ is of great assistance when MOSFETs are paralleled. It is possible, in DC applications, to parallel devices without any matching, and those devices that initially draw the most current will heat up and shift the current to other devices to more equally distribute the current. This is exactly the opposite of the scenario for bipolar devices. While the paralleling of unmatched devices will work, it is a poor idea because a higher than necessary dissipation may occur, and in switching applications it is possible for one device to turn on or off before or after the others, and to have to accept the full load current. This may force the device to function outside of its safe operating area.

It is recommended that the user parallel devices which have been matched for V_{th} to within 5%. This will assure that the turn-on and turn-off delays due to the gate voltage rise and fall times, relative to V_{th}, are nearly equal. The values for $r_{DS(ON)}$ will also be very close, so that excessive differential heating is not encountered. Some additional improvement in $r_{DS(ON)}$ matching may be achieved by providing higher V_{GS} so that all of the parallel devices run at their minimum $r_{DS(ON)}$ value.

It should be kept in mind that many MOSFET devices have gain bandwidth products over 500MHz. It is entirely possible for these devices to oscillate at very high frequencies, especially if multiple parallel devices are used. This is often an unsuspected cause of device failure. If the circuit designer is using a low-bandwidth oscilloscope during breadboard development, it is possible to be unaware of the self oscillation, and therefore the use of an oscilloscope with a bandwidth of at least 200MHz is recommended. The tendency towards oscillation can be greatly reduced by inserting ferrite beads or low-value (50-100Ω) resistors in series with the gate leads, as shown in Figure 54.

For fast pulse applications, it is not sufficient to merely match the devices. The circuit must also be reasonably symmetrical so that identical drive voltages are applied to each gate. At high speeds the inductive as well as resistive effects must be considered. If, for example, the parasitic inductance in the drain lead of Q_1 is much smaller than that in the drain lead of Q_N, when the devices are first turned ON most of the load current will initially flow through Q_1, even if the gate drives and threshold voltages are identical.

Variations in the stray gate circuit capacitance and the device input capacitance can also cause uneven turn-on in fast pulse applications. The effect of this can be reduced by equalizing the stray capacitance and minimizing the intergate impedances. For applications requiring switching times below 10ns, it may be necessary to match the device capacitances.

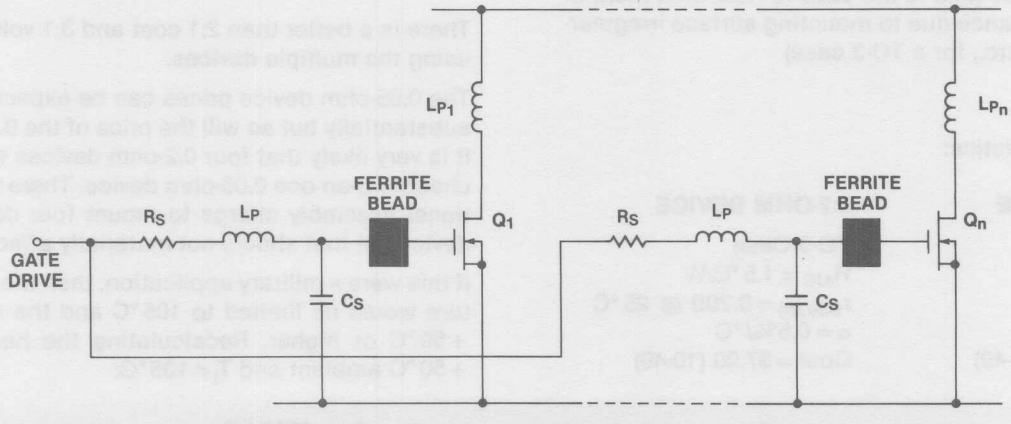


Figure 54. Parallel Devices

It should be kept in mind that most of the complications in paralleling mentioned above apply only for very fast pulses. Most applications will use transition times well above 10ns, where simple threshold voltage matching is all that is required. This is quite different from bipolar devices where paralleling more than two devices can become quite complex and expensive. Due to the practical difficulties of paralleling large numbers of individual bipolars, (and SCRs also), the trend has been to develop ever larger single devices. As the die size increases, a point is reached where either the thermal capabilities or the available mounting areas of the low-cost packages are exceeded so that a more expensive package is required. In addition the heat sink will now see a concentrated thermal input through the relatively small package to heat sink contact area. The efficiency of a heat sink is better if the heat input is distributed in several sources rather than in one.

While the arguments for using a single large bipolar device instead of multiple smaller devices are well founded, it does not necessarily follow that the same technique should be imitated in power MOSFET devices, especially in the light of the rapid cost increase of the larger die. The tradeoff may well be multiple devices with low die and package and moderate heat sink costs, versus single devices with high die, package and heat sink costs. Just where the cost crossover point between single and multiple devices is has yet to be determined, especially since the very high prices for the present larger MOSFETs are certain to be reduced substantially.

The following design example illustrates the thermal arguments for paralleling devices.

Statement of the Problem:

Solve for the heat sink area, volume, and cost and the combined heat sink and device cost. Compare one 0.05-ohm device to four 0.2-ohm devices.

Operating Conditions:

I_D = 25A RMS
T_a = 40 °C
T_{jmax} = 150 °C
Altitude = Sea level
Cooling = Still air convection cooling
$R_{\theta CH}$ = 0.4 °C/W (this is the case to heat sink thermal impedance due to mounting surface irregularities, etc., for a TO-3 case)

Device Characteristics:

0.05-OHM DEVICE

TO-3 Case
$R_{\theta JC} = 0.83$ °C/W
$r_{DS(ON)} = 0.05\Omega$
$\alpha = 0.5\%/°C$
Cost = $62.20 (10-49)

0.2-OHM DEVICE

TO-3 Case
$R_{\theta JC} = 1.5$ °C/W
$r_{DS(ON)} = 0.20\Omega$ @ 25 °C
$\alpha = 0.5\%/°C$
Cost = $7.00 (10-49)

For this problem the device power dissipation, P, and heat sink area, A, can be shown (see appendix) to be:

$$A = \left[\frac{80P^{0.85}}{T_j - T_a - P\,R_{\theta CH}}\right]^{1.43} \quad (39)$$

$$P = r_{DS(ON)}\, e^{\alpha \cdot \Delta T} \quad (40)$$

(Note: Equation 40 is equivalent to Equation 12.)

Calculations:

One 0.05-Ohm device:

$$P = (0.05)\,(25^2)e^{(0.005)\,(110)} = 54.2W$$

$$\theta_{j-hs} = R_{\theta JC} + R_{\theta CH} = 0.83 + 0.4 = 1.23\,°C/W$$

$$A = \left[\frac{80(54.2)^{0.85}}{110 - 54.2(1.23)}\right]^{1.43} = 308\ in^2$$

Because the heat input is concentrated, the heat sink will be less efficient by 10 to 30% than calculated. For a 20% loss in efficiency:

$$A_1 = 370\ in^2$$

Four 0.2-Ohm devices:

$$P = 54.2W$$

$$R_{\theta CH} = \frac{1.5 + 0.4}{4} = 0.48\,°C/W$$

$$A_2 = \left[\frac{80(54.2)^{0.85}}{110 - 54.2(0.48)}\right]^{1.43} = 120\ in^2$$

Using the AHAM #4501 heat sink extrusion ($A = 28\ in^2/in$) the heat sink length, L, and volume, V, are:

$L_1 = 13.2$ in $L_2 = 4.3$ in
$V_1 = 64\ in^3$ $V_2 = 21\ in^3$
$V_1/V_2 = 3.1!$

A 72″ section of this heat sink costs about $80, so:

$C_1 = \$14.67$
$C_2 = \$\ 4.78$

Total Costs: One 0.05-ohm device = $76.87
Four 0.2-ohm devices = $32.78

There is a better than 2:1 cost and 3:1 volume advantage to using the multiple devices.

The 0.05-ohm device prices can be expected to come down substantially but so will the price of the 0.2-ohm devices, so it is very likely that four 0.2-ohm devices will continue to be cheaper than one 0.05-ohm device. There will be some additional assembly charge to mount four devices versus one device but that should not materially affect the comparison.

If this were a military application, then the junction temperature would be limited to 105 °C and the ambient would be +50 °C or higher. Recalculating the heat sink areas for +50 °C ambient and $T_j \neq 105$ °C:

$A_1 = 1503\ in^2$
$A_2 = 227\ in^2$
$A_1/A_2 = 6.62!$

By no means does the design example imply that multiple devices are **always** superior to a single device. The tradeoff will depend on device costs and cooling provisions, and the tradeoff will take the general form shown in Figure 55. In some situations the additional volume of the multiple packages may be a problem. In most cases, however, this should not be a concern. It can also be argued that the increased number of devices reduces the reliability. The counter argument to this is that multiple devices can be run cooler due to the improved thermal efficiency and the net reliability is actually increased.

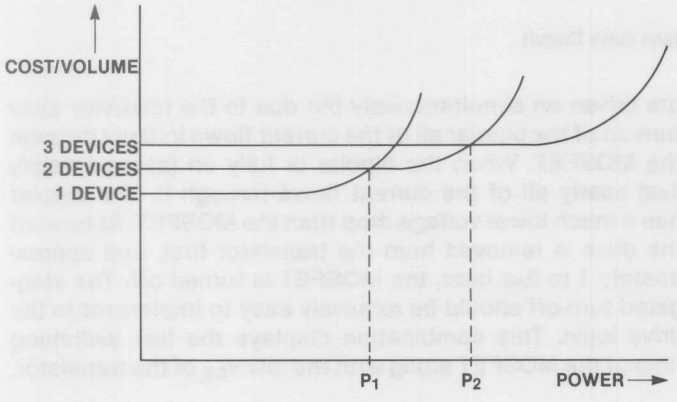


Figure 55. Cost versus Power Dissipation

Series Operation MOSFETs

MOSFETs can be connected in series for high-voltage operation. It is particularly important that all devices in the same series string come ON simultaneously, otherwise one device may take all of the voltage momentarily. The devices should be well matched for V_{th} and careful attention given to producing simultaneous gate drive. In those applications where the maximum possible voltage capability is desired, it may be necessary to match the $r_{DS(ON)}/V_{GS}$ characteristic to assure equal voltage distribution during switching transitions. This is a much more complex procedure than V_{th} matching, and should be considered only as a last resort. It is probably preferable to use some form of snubber network to equalize the voltage distribution during switching. Analogous to the parasitic inductance in parallel operation is the effect of circuit parasitic capacitance in series operation. If differential drain-source capacitances (either in the device or in the circuit layout) exist in the series string, the transient voltages may not be shared equally.

Combinations of Bipolar Transistors and MOSFETs

MOSFETs can be combined with transistors in a variety of useful ways. The most obvious combination is to use medium-power MOSFETs to drive high-power bipolars; the MOSFET is an excellent buffer between TTL or CMOS logic and large bipolar devices.

Two base drive possibilities are given in Figure 56. In (B) R_1 and R_2 are selected independently to provide the appropriate values for I_{B1} and I_{B2}. If negative bias for Q_3 is desired, the source of Q_2 and the ground pin of the DS0026 may be referenced to a negative potential. Figure 57 shows a proportional[5] base drive circuit.

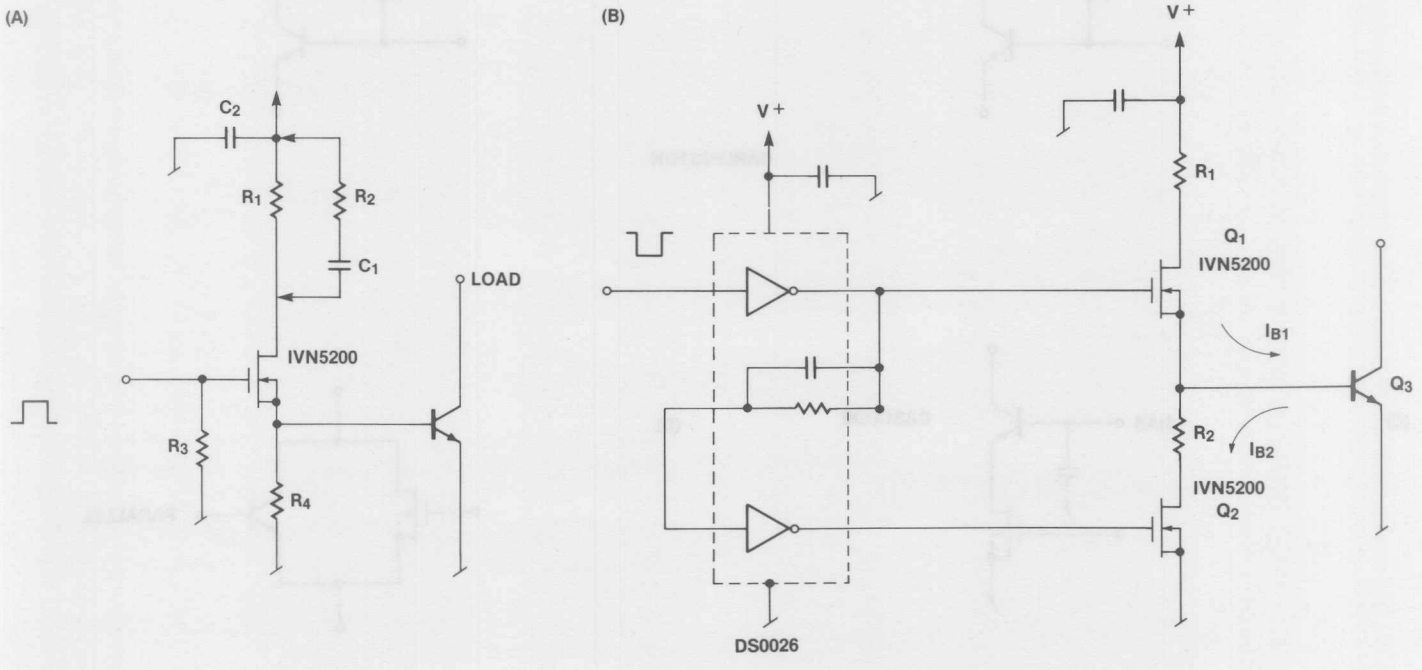


Figure 56. Bipolar Base Drive Using MOSFET

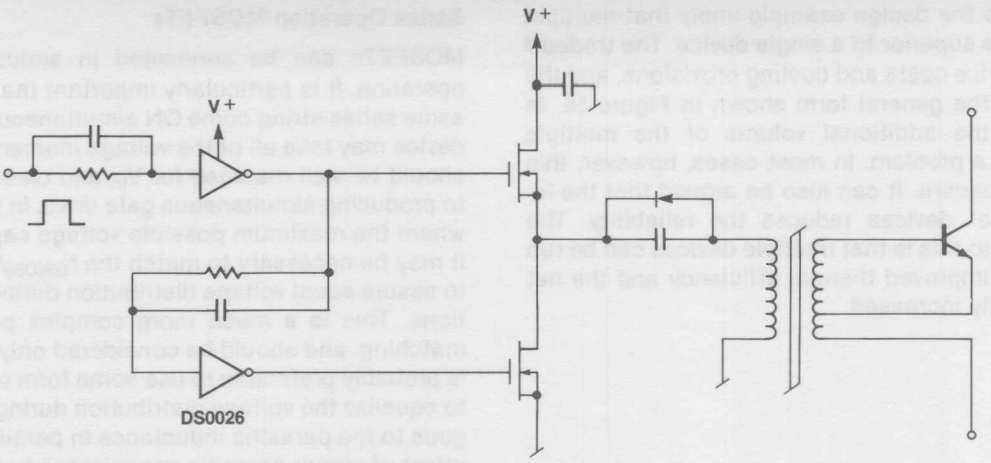


Figure 57. Proportional Base Drive Circuit

In addition to using MOSFETs to drive bipolar transistors, the two types of devices may be combined into a compound device. Some of the possibilities are shown in Figure 58. The Darlington connection (58A and 58B) using a MOSFET for the driver will display essentially infinite beta. The cascade connection shown in Figures 58C, 59 and 60 is a means to obtain fast switching from a large high-voltage bipolar by inserting a low-voltage, low-$r_{DS(ON)}$ MOSFET in the emitter.

Another interesting possibility is to parallel a MOSFET and a larger bipolar transistor. The MOSFET and the transistor are driven on simultaneously but due to the relatively slow turn-on of the bipolar all of the current flows initially through the MOSFET. When the bipolar is fully on (approximately 1μs) nearly all of the current flows through it. The bipolar has a much lower voltage drop than the MOSFET. At turn-off the drive is removed from the transistor first, and approximately 1 to 3μs later, the MOSFET is turned off. The staggered turn-off should be relatively easy to implement in the drive logic. This combination displays the fast switching time of the MOSFET along with the low V_{CE} of the transistor.

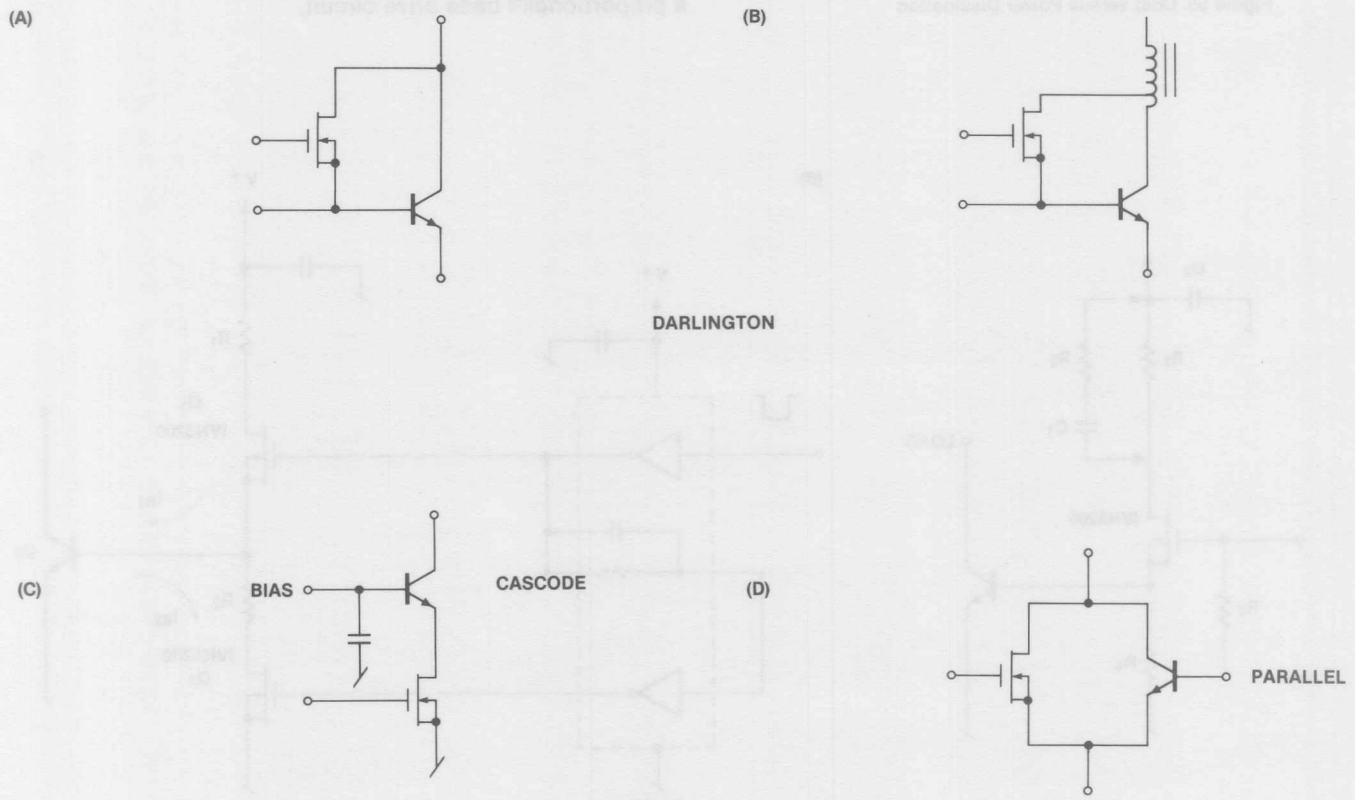


Figure 58. BJT/MOSFET Combinations

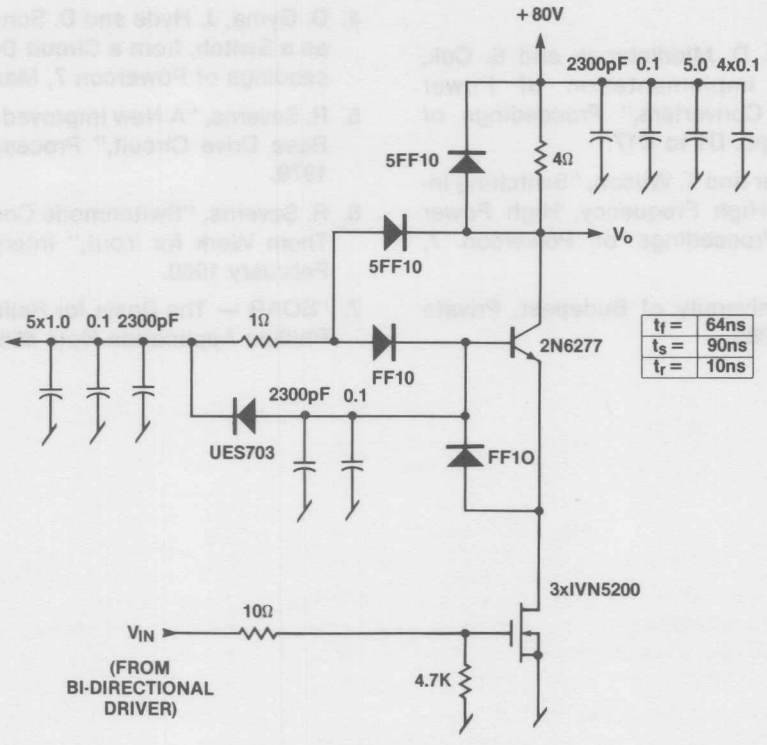


Figure 59. Cascode BJT/MOSFET Circuit

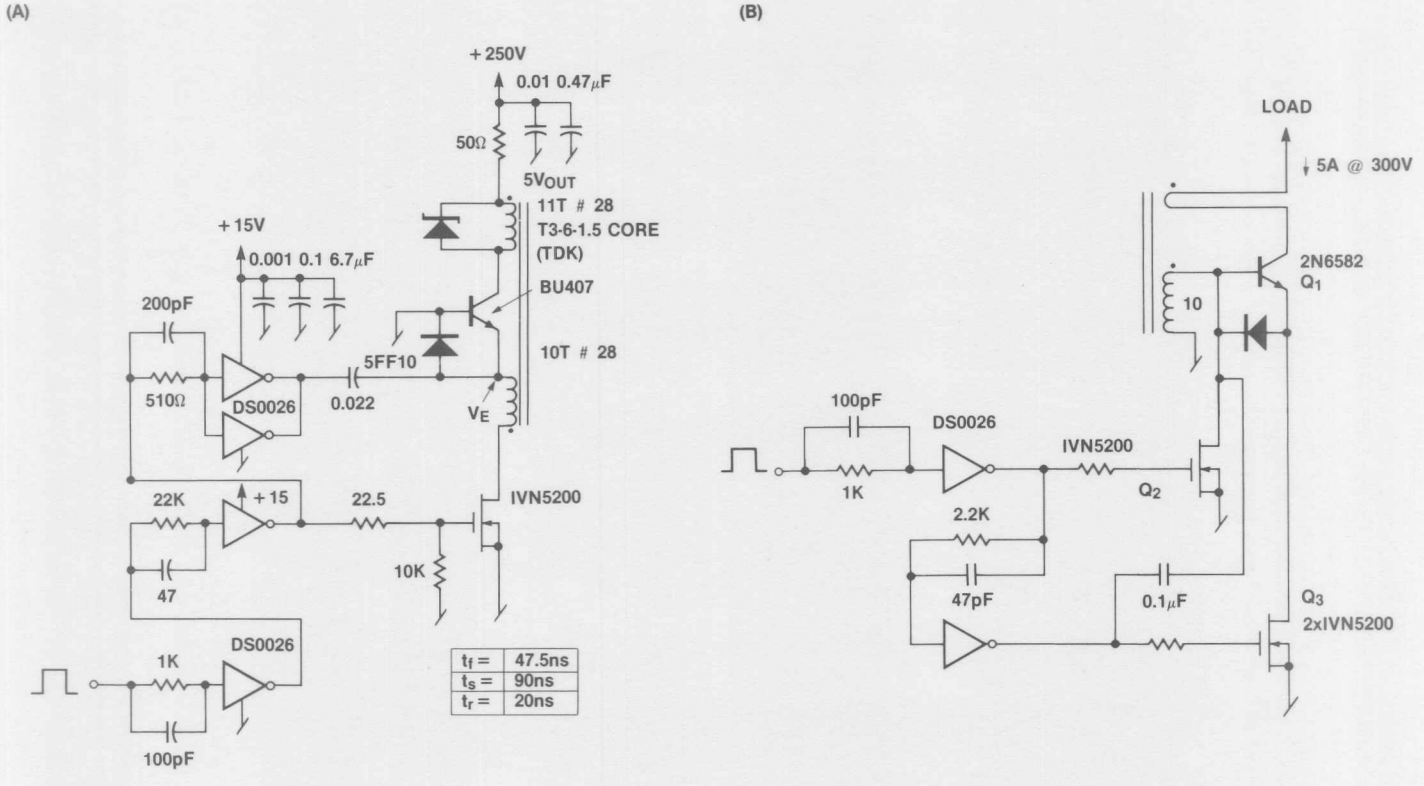


Figure 60. Proportionally Driven Cascode BJT/MOSFET

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SELECTOR GUIDE N-CHANNEL ENHANCEMENT MODE VERTICAL POWER MOS $BV_{DSS} < 100V$

$r_{DS(on)}$ OHMS	$I_{D(on)}$ AMPS		$V_{GS(th)}$ VOLTS		P_D WATTS $T_C = 25°C$	BV_{DSS} — DRAIN-SOURCE BREAKDOWN VOLTAGE										PACKAGE
						35V MIN		40V MIN		60V MIN		80V MIN		90V MIN		
MAX	STEADY	PEAK	MIN	MAX	MIN	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	
0.5	5.0	12	0.8	2.0	50				IVN5200KND		IVN5200KNE		IVN5200KNF			TO-3
0.5	5.0	12	0.8	3.6	50				IVN5201KND		IVN5201KNE		IVN5201KNF			
0.5	4.0	10	0.8	2.0	12.5				IVN5200TND		IVN5200TNE		IVN5200TNF			
0.5	4.0	10	0.8	3.6	12.5				IVN5201TND		IVN5201TNE		IVN5201TNF			
2.5	1.2	3.0	0.8	2.0	6.25		VN35AK		IVN5000TND		IVN5000TNE		IVN5000TNF		IVN5000TNG	
2.5	1.2	3.0	0.8	—	6.25	VN35AB			IVN5001TND		IVN5001TNE		IVN5001TNF		IVN5001TNG	
3.0	1.2	3.0	0.8	2.0	6.25					IVN6660	VN66AK					TO-39
3.5	1.2	3.0	0.8	2.0	6.25						VN67AK					
3.5	1.2	3.0	0.8	—	6.25					VN67AB						
4.0	1.2	3.0	0.8	2.0	6.25									IVN6661	VN98AK	
4.5	1.2	3.0	0.8	2.0	6.25										VN99AK	
4.5	1.2	3.0	0.8	—	6.25							VN89AB				
5.0	1.2	3.0	0.8	—	6.25	VN30AB								VN90AB		
2.5	0.9	3.0	0.8	2.0	3.13				IVN5000SND		IVN5000SNE		IVN5000SNF			TO-52
2.5	0.9	3.0	0.8	3.6	3.13				IVN5001SND		IVN5001SNE		IVN5001SNF			
0.5	5.0	12	0.8	2.0	30				IVN5200HND		IVN5200HNE		IVN5200HNF			TO-66
0.5	5.0	12	0.8	3.6	30				IVN5201HND		IVN5201HNE		IVN5201HNF			
3.0	1.7	3.0	0.8	—	12			VN46AF		VN66AF						
3.5	1.7	3.0	0.8	—	12					VN67AF						
4.0	1.7	3.0	0.8	—	12							VN88AF				
4.5	1.7	3.0	0.8	—	12							VN89AF				TO-202 (PLASTIC)
5.0	1.7	3.0	0.8	—	12			VN40AF								
2.5	1.7	3.0	0.8	2.0	12				IVN5000BND		IVN5000BNE		IVN5000BNF			
2.5	1.7	3.0	0.8	3.6	12				IVN5001BND		IVN5001BNE		IVN5001BNF			
0.5	5.0	12	0.8	3.6	30				IVN5201CND		IVN5201CNE		IVN5201CNF			TO-220 (PLASTIC)
2.5	0.7	2.0	0.8	2.0	2.0				IVN5000AND		IVN5000ANE		IVN5000ANF			
2.5	0.7	2.0	0.8	3.6	2.0				IVN5001AND		IVN5001ANE		IVN5001ANF			TO-237 (PLASTIC)
—	0.5	1.0	0.3	2.5	1.0					VN10KM						
3.0	0.5	2.0	0.8	3.6	2.0					IVN5001AZE		IVN5001AZF				

$R_{DS(on)}$ OHMS	$I_{D(on)}$ AMPS		$V_{GS(th)}$ VOLTS		P_D WATTS $T_C = 25°C$	BV_{DSS}		
MAX	STEADY	PEAK	MIN	MAX	MIN	350V	400V	450V
3.0	2.25	7.5	2.0	5.0	36	IVN6000KNR	IVN6000KNS	IVN6000KNT

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